

Lateral Discrete Power MOSFET: Enabling Technology for Next-Generation, MHz-Frequency, High-Density DC/DC Converters

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Abstract—DC/DC converters to power future CPU or DSP cores mandate low-voltage power MOSFETs with ultra low on-resistance and gate charge. Conventional trench MOSFETs cannot meet the challenge. We introduce an alternative device technology, the discrete lateral power MOSFETs, to overcome the limitations associated with the vertical trench or planar MOSFETs. We report a family of 7V, 20V, and 30V lateral discrete power MOSFETs with figures of merit 2-3 times better than the state-of-the-art trench MOSFETs. We have developed an innovative metal interconnect and chip-scale packaging approach to overcome the “scaling barrier” which limits the chip size and current rating of the traditional lateral power devices. The lateral MOSFETs were designed and fabricated with a simplified CMOS process, and packaged in flip-chip forms using a wafer bumping technology. Lateral discrete power MOSFETs will become a viable enabling technology for next-generation, MHz-frequency, high-density DC/DC converters.

Index Terms—Power MOSFET, DC/DC converter, synchronous rectifier, distributed power architecture.

I. INTRODUCTION

MICROPROCESSOR core voltages continue to decrease as IC fabrication technology advances. At the same time, the power and current consumption continue to increase as new functions and more transistors are integrated into the chip. According to the Semiconductor Industry Association (SIA) technology roadmap, IC chips will be operating less than 1V, drawing up to 170A by 2005 [1]. This will impose a very small tolerance window for voltage regulation if similar percentage tolerance for high bus voltages is maintained. In addition, the increase in CPU operating frequency and the use of on-chip active power management techniques such as clock gating and thermal throttling require a higher current slew rate or di/dt. The requirements for accurate voltage regulation and fast transient response drive up the need for advanced DC/DC converters with high efficiency, high power density, and a switching frequency well above 1MHz. This in turn poses significant challenges to all components, specially the power

MOSFETs, of the DC/DC converter.

The maximum switching frequency of a power MOSFET is mainly limited by its gate charge and switching losses as well as the ability to control short on times. Power MOSFETs, serving as both the main control switch and the synchronous rectifier in various MHz-frequency DC/DC converter topologies, need to be optimized for the gate charge and capacitance, gate resistance, output capacitance, and on-resistance $R_{DS(ON)}$. Currently trench MOSFETs are predominantly used in DC/DC converter applications [2]-[4]. Trench MOSFETs offer a very low specific $R_{DS(ON)}$ for voltage ratings between 20 and 80 volts, and are well suited for DC/DC applications with a switching frequency up to several hundred kHz. However, trench MOSFETs suffer from high gate charge and capacitance due to the inherent vertical trench gate structure. Recently efforts have been made to reduce the gate charge of trench MOSFET with some penalty on $R_{DS(ON)}$ [5], [6]. However, it is uncertain if these incremental improvements are sufficient to make trench MOSFETs a viable solution for multi-megahertz switching applications.

As both the output and input voltages of DC/DC converters continue to decrease, the voltage rating of the synchronous rectifier MOSFETs for many applications can be reduced to 15-5V. Within this voltage range, the parasitic resistance from device substrate and package becomes dominant. The low channel resistance of trench MOSFET's is no longer a differentiating factor when competing with other device technologies. Furthermore, vertical power MOSFETs, trench or planar alike, are typically packaged in industry-standard, wire bond, surface-mount packages such as SO-8, D-PAK, or MLP packages [7]. While these packages offer low cost benefits, they no longer meet the requirements of low parasitic impedance, small package footprint, low package profile for high power density, MHz-frequency DC/DC converters. As the MOSFET chip size continuously shrinks for lower gate charge and cost, it becomes increasingly difficult to remove heat from the silicon housed in these packages.

In this paper, we introduce an alternative device solution, the discrete lateral power MOSFETs, to overcome the aforementioned limitations associated with the vertical trench or planar MOSFET technology and meet the stringent requirements for next-generation, MHz-frequency, high-density DC/DC converters. We introduce a series of lateral discrete power MOSFETs with voltage ratings of 7V, 20V, and 30V. The performance figures of merit (FOM) of these lateral MOSFETs range from 2-3 times better than the state-of-the-art trench MOSFETs with the same voltage rating. These lateral MOSFETs were designed and fabricated with a simplified CMOS process, and packaged in flip-chip forms using a well established wafer bumping technology.

II. MOSFET POWER LOSSES IN DC/DC CONVERTERS

There are various DC/DC converter topologies including both isolated and non-isolated types. Power MOSFETs are usually used as both the main control switch and the synchronous rectifier. Detailed power loss analysis depends on the specific circuit topology and control scheme used in the converter. A simple synchronous Buck converter is often used to help understanding the power losses of power MOSFETs, as shown in Fig. 1.

The synchronous Buck converter uses two power MOSFETs – a high-side control FET Q1 and a low-side synchronous FET Q2. A PWM control IC alternately switches the two MOSFETs Q1 and Q2. The PWM switching duty cycle determines the converter output voltage. The power losses of the control FET Q1 can be calculated as follows [4], [8]:

$$\begin{aligned}
 P_{Q1} &= P_{COND} + P_{SW} + P_{GD} + P_{OSS} \\
 P_{CON} &= I_{rms}^2 R_{DS(ON)} \\
 P_{SW} &= \frac{I_o}{I_G} V_{in} (Q_{gs2} + Q_{gd}) f_s \\
 P_{GD} &= Q_g V_g f_s \\
 P_{OSS} &= \frac{1}{2} V_{in} Q_{OSS} f_s
 \end{aligned}$$

where P_{COND} is the conduction loss, P_{SW} is the switching loss, P_{GD} is the gate drive loss, and P_{OSS} is the loss associated with the output charge of Q1. Q_g is the total gate charge, Q_{gd} is the gate-drain charge and Q_{gs2} is one part of the total gate-source

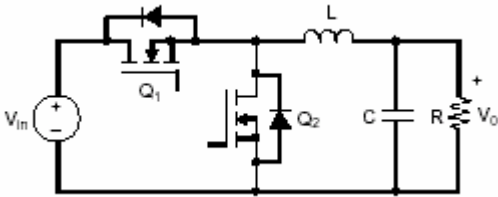


Fig. 1. A synchronous Buck converter.

charge. f_s is the PWM switching frequency.

Similarly the power losses of the synchronous FET Q2 can be calculated as follows:

$$\begin{aligned}
 P_{Q1} &= P_{COND} + P_{GD} + P_{OSS} + P_{Qrr} \\
 P_{CON} &= I_{rms}^2 R_{DS(ON)} \\
 P_{GD} &= Q_g V_g f_s \\
 P_{OSS} &= \frac{1}{2} V_{in} Q_{OSS} f_s \\
 P_{Qrr} &= V_{in} Q_{rr} f_s
 \end{aligned}$$

where P_{Qrr} is the power loss generated by the diode reverse recovery charge Q_{rr} . Note that the conduction loss of Q2 is the same as for Q1 but the Q2 switching loss is negligible since the synchronous FET is zero-voltage switching.

As seen from the above power loss calculation, the on-state resistance $R_{DS(ON)}$ and gate charge Q_g of the power MOSFET both contribute to the total power losses. While $R_{DS(ON)}$ traditionally dominates the total power losses at low PWM switching frequencies, Q_g is becoming more dominant as the converter switching frequency is raised to multi-megahertz to improve the transient response and miniaturize the passive components. Power MOSFET design is now being focused on the trade-off between the conduction loss, switching loss, and the gate drive loss. A simple indicator of the device performance of a power MOSFET for DC/DC converter applications is the figure of merit (FOM) defined as

$$FOM = R_{DS(ON)} \times Q_g$$

A small FOM of the power MOSFET generally leads to a high DC/DC converter operation efficiency.

III. VERTICAL VS. LATERAL POWER MOSFETs

Vertical trench MOSFETs, which currently dominate the DC/DC converter market, offer very low specific $R_{DS(ON)}$, but suffer from high gate charge and gate capacitance due to the inherent vertical trench gate structure. As the output/input voltages of DC/DC converters continue to decrease, the voltage rating of the synchronous rectifier MOSFETs for many applications can be reduced to below 10V. Within this voltage range, the low channel resistance of trench MOSFET's is overshadowed by the parasitic resistance from the device substrate and package (mainly wirebonds).

The concept of lateral power MOSFETs is not new. It was extensively studied long before the trench MOSFET technology became commercially successful a decade ago. However, until recently lateral MOSFETs were exclusively used in smart power ICs or as discrete RF devices [9]. Lateral discrete MOSFETs are generally not considered sufficiently cost-effective for high current switching power applications. Figure 2 illustrates the device cross-sectional views of a vertical trench MOSFET and a lateral N-channel MOSFET. The parasitic gate-drain capacitance C_{gd} (the Miller capacitance) is also labeled in both devices. It is evident that the lateral MOSFET inherently has a much smaller overlap

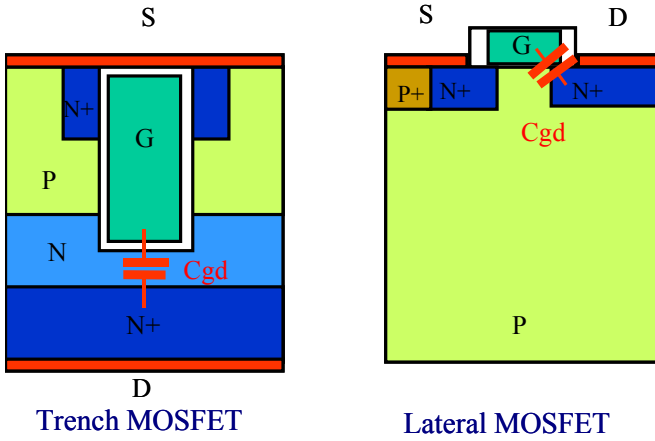


Fig. 2. Cross-sectional views of vertical trench MOSFET and lateral N-channel MOSFET with gate-drain capacitance C_{gd} labeled.

area between its polysilicon gate electrode and N+ drain than the trench MOSFET, and therefore offers a much lower gate capacitance and gate charge.

Lateral power MOSFETs used to suffer from relatively high on-resistance since the current flows horizontally along the silicon surface, not as effective as vertical trench MOSFETs in terms of silicon utilization. However, the on-resistance of lateral MOSFETs has been improved significantly during the last few years [9]. Now the difference in specific $R_{DS(ON)}$ between lateral and trench MOSFETs is only in the range of 10-30% depending on the voltage rating. This factor, in conjunction with an ultra-low gate charge and capacitance, makes the lateral MOSFETs extremely suitable in the high-frequency DC/DC converters [10]-[13].

However, the $R_{DS(ON)}$ of conventional lateral MOSFETs deteriorates considerably with increasing device size due to the parasitic resistance of metal interconnects, commonly known as the “scaling issue” [14]. Interconnect resistance does not only add to drain/source series resistance but also causes a “debiasing” effect in active device cells, as shown in Fig. 3. This imposes a fundamental limit on the maximum die size practically achievable by lateral device structures. This is the main reason why most smart power ICs only offer a limited power and current rating. This technical barrier needs to be overcome before lateral discrete MOSFETs become a viable solution for high current DC/DC converter applications.

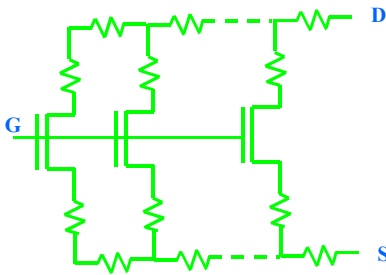


Fig. 3. The effect of metal interconnect resistance on lateral MOSFET.

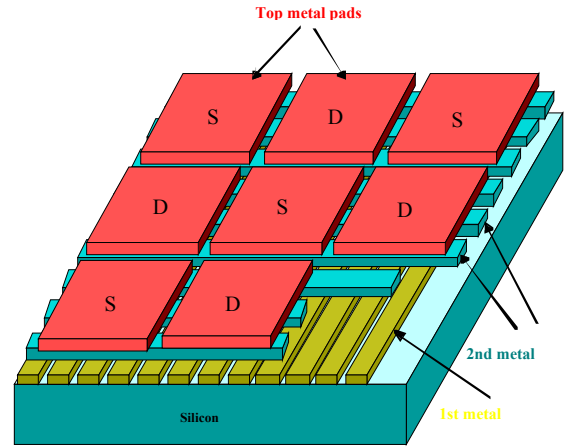


Fig. 4. Multi-layer metal interconnect scheme to reduce parasitic resistance of lateral power MOSFETs.

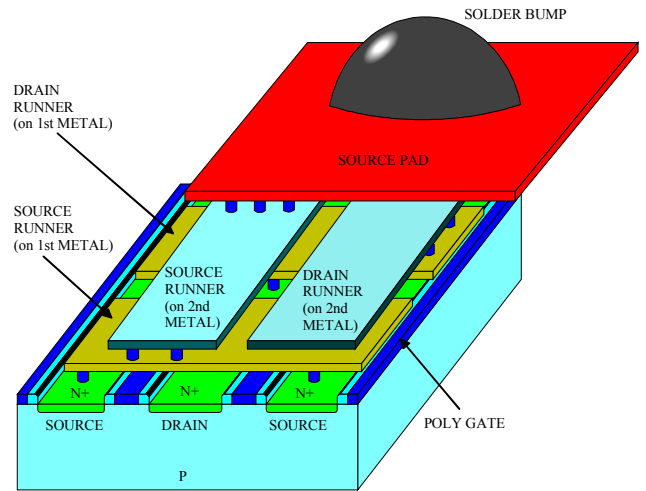


Fig. 5. Detailed 3-layer metal interconnect scheme to reduce parasitic resistance of lateral power MOSFETs (Only one SOURCE pad is shown).

IV. METAL INTERCONNECT AND CHIP-SCALE PACKAGING INNOVATION

In this paper, we introduce an innovative metal interconnect and chip-scale packaging concept to overcome the lateral scaling limitation by integrating standard CMOS and wafer bumping processes [15]. Figure 4 illustrates the basic device concept. A large area lateral MOSFET is formed in silicon with source, drain, and gate regions (details not shown). Multiple source and drain pads are formed in the top metal layer of three-layer metal interconnect scheme. These source, drain, and gate (not shown) pads are of approximately $500\mu\text{m}$ by $500\mu\text{m}$. Single- or double-layer metal runners can be used to interconnect the source, drain, and gate regions in the silicon chip to the top metal pads, as shown in more detail in Fig. 5. The source and drain top metal pads are arranged in a checkerboard or interleaved pattern to guarantee that any active cells in the silicon chip have access to one of the source or drain pads within a short distance such as $250\mu\text{m}$. Solder

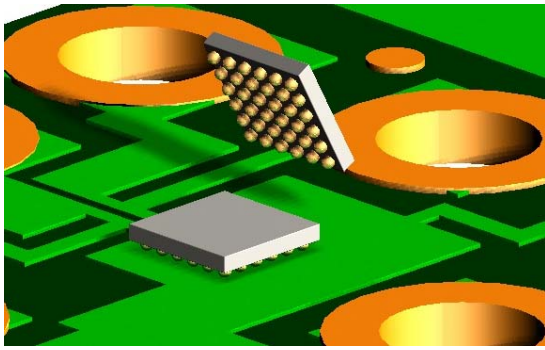


Fig. 6. Concept of the flip chip power MOSFET being mounted on PCB.

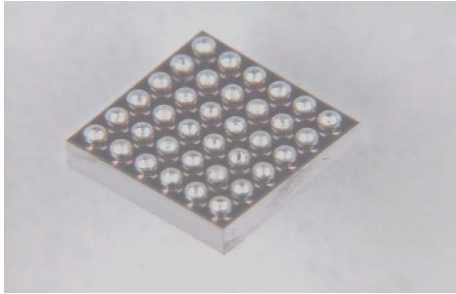


Fig. 7. Actual photo picture of the flip-chip lateral power MOSFET (dimensions: $3.175 \times 3.175 \text{mm}^2$).

bumps are subsequently applied to all source/drain/gate pads using a wafer bumping technique. The finished flip chip MOSFET is then assembled on a printed circuit board (PCB) similarly to a conventional surface mount device, as shown in Fig. 6. The single- or multi-layer thick copper films of the PCB effectively connect all drains and sources in parallel. Figure 7 shows an actual photo picture of a flip-chip lateral MOSFET with a die size of 3.175mm by 3.175mm .

Flip chip or chip scale packages (CSP) offer the solution for miniaturization using conventional surface mount (SMT) assembly equipment, and are gaining tremendous market acceptance in the last few years. CSP is a true chip size package in which the package size is the die size. One attractive feature of this package is its wafer level fabrication process, which offers significant cost reduction comparing with die-level CSP technologies or BGA packages using copper carriers.

A standard SMT process can be used to assemble the CSP power MOSFET. The standard process flow consists of screen printed solder paste, placement with a chip shooter or a fine-pitch component placement tool and reflow in a conventional oven. Currently there are three important factors that influence the industry-wide acceptance of CSP packages: cost, reliability and board technology development.

V. DEVICE PERFORMANCE

A $0.5 \mu\text{m}$ simplified CMOS process including 3 or 2 metal layers is used to fabricate the new device. Depending on the targeted breakdown voltage rating, various lateral MOSFET structures are adopted, including LDD NMOS and LDMOS structures. A series of lateral power MOSFETs with voltage

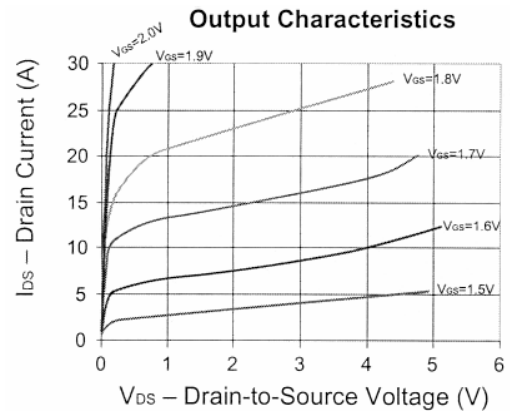


Fig. 8. GWS24N07CS output characteristics.

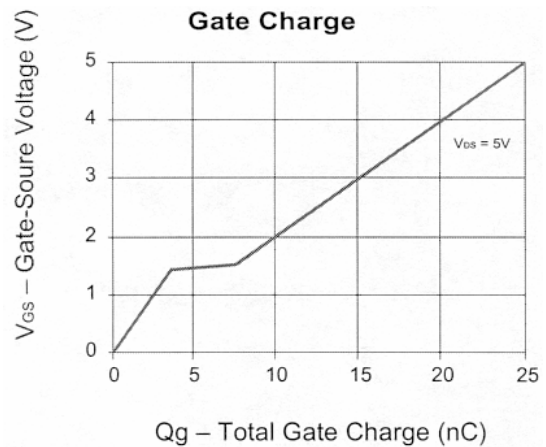


Fig. 9. GWS24N07CS gate charge characteristics.

ratings of 7V, 20V, and 30V were designed and fabricated based on the previously described interconnect and chip-scale packaging concept. A chip size of $3.175 \times 3.175 \text{mm}^2$ is used for all these devices. The devices have been characterized electrically. Critical device parameters such as on-resistance $R_{\text{DS(ON)}}$, gate charge Q_g , gate resistance R_g , and figure of merit (FOM) $R_{\text{DS(ON)}} \times Q_g$ are discussed as the following.

The first device to be reported is GWS24N07CS, an N-channel power MOSFET rated at 7V and 24A. This device demonstrates a record low $R_{\text{DS(ON)}}$ of $1 \text{m}\Omega$ at a gate voltage of 6V, or $1.25 \text{m}\Omega$ at a gate voltage of 4.5V, approximately 50% of the lowest $R_{\text{DS(ON)}}$ previously reported for a single packaged power MOSFET [16]. This low $R_{\text{DS(ON)}}$ is actually measured with the MOSFET mounted on the PCB, and therefore includes all possible parasitic resistance. The new device has a total gate charge Q_g of 22nC at 4.5V and a performance FOM less than $30 \text{m}\Omega \cdot \text{nC}$. This represents an improvement of factor-of-three over the state of the art trench MOSFETs. The new MOSFET has a breakdown voltage of 11V and is suitable for sub-10V class DC/DC applications. The MOSFET has also demonstrated an ultra-low gate resistance of 0.4Ω . Figures 8 and 9 show the I-V and gate charge characteristics of the new MOSFET respectively. The new MOSFET is also compared to a state of the art commercial trench MOSFET [16] and a previously reported lateral MOSFET [10] in Table I.

TABLE I
DEVICE PERFORMANCE OF GWS24N07

Device Parameters	GWS24N07 (This work)	Trench MOSFET (Si4838DY)	LDD NMOS (Prior work [10])
BV_{DSS} (V)	11	12	7.4
V_{th} (V)	1.0	0.6	0.55
$R_{dson @4.5V}$ (m Ω)	1.25	2.4	6
$Q_g @4.5V$ (nC)	22	40	3.8
FOM (m Ω *nC)	27.5	96	22.8
R_g (Ω)	0.4	1.7	N/A
Package Footprint (mm ²)	9.5 (chip-scale)	32 (SO-8)	N/A

TABLE II
DEVICE PERFORMANCE OF GWS12N20

Device Parameters	Lateral MOS GWS12N20	Trench MOSFET (Si7882DP)	Trench MOSFET (IRF6601)
BV_{DSS} (V)	27	>20	>20
$R_{dson @4.5V}$ (m Ω)	4.4	5.4	4.4
$Q_g @4.5V$ (nC)	18	38	30
FOM (m Ω *nC)	79.2	205	132
R_g (Ω)	0.4	0.9	N/A
Package Footprint (mm ²)	9.5 (chip-scale)	31.5 (PowerPAK SO-8)	32 (DirectFET)

TABLE III
DEVICE PERFORMANCE OF GWS10N30

Device Parameters	GWS12N20	Trench MOSFET (Si7894DP)	Trench MOSFET (IRF6608)
BV_{DSS} (V)	38	>30	>30
$R_{dson @4.5V}$ (m Ω)	5.5	4.4	8
$Q_g @4.5V$ (nC)	16	48	16
FOM (m Ω *nC)	88	211	128
R_g (Ω)	0.4	1.3	N/A
Package Footprint (mm ²)	9.5 (chip-scale)	31.5 (PowerPAK SO-8)	19 (DirectFET)

GWS24N07CS was successfully adapted in a 200W DC/DC converter operating at 3.5MHz and 97-99% efficiency. An amazing 800W/in³ power density was achieved.

The second device to be reported is GWS12N20, an N-channel LDMOS transistor rated at 20V and 12A. The performance of GWS12N20 is summarized and compared to two 20V commercial trench MOSFETs in Table II. The third device we report is GWS10N30, an N-channel LDMOS transistor rated at 30V and 10A. The performance of GWS10N30 is summarized and compared to two 30V commercial trench MOSFETs in Table III. It is observed that the flip-chip lateral discrete MOSFETs demonstrate specific $R_{DS(on)}$ comparable to trench MOSFETs and much lower gate charge and superior performance FOM.

VI. CONCLUSION

Lateral discrete power MOSFETs in chip scale packages offer ultra-low gate charge and capacitance, competitive on-resistance for voltage ratings above 20V and unmatched low on-resistance below 20V, and performance figures of merit superior to the state-of-the-art trench MOSFETs. We have developed an innovative metal interconnect and chip-scale packaging approach to overcome the “scaling barrier” which limits the chip size and current rating of traditional lateral power devices. In addition to its superior on-resistance and gate charge performance, the flip-chip lateral MOSFETs offer very low parasitic package resistance and inductance for better efficiency and low EMI as well as top-side (junction side) cooling capability. The chip scale package also provides a much smaller footprint than conventional packages to save precious board space. The lateral discrete MOSFETs can be fabricated with standard CMOS processes and thus result in great cost benefits [17]. Future work includes improving device avalanche capability and ruggedness and extending the voltage rating to even a higher level. The basic metal interconnect and chip scale package concepts presented in this paper can also be applied to smart power ICs to significantly increase their power ratings. In summary, lateral discrete power MOSFETs will become a viable enabling technology for the next-generation, MHz-frequency, high-density DC/DC converters to power up personal computers, servers, and telecom equipment.

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