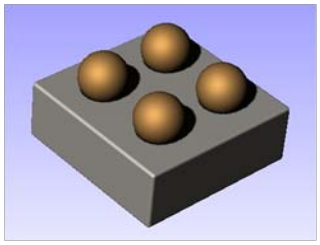
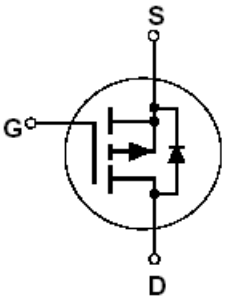
GWS8405P - Single P-Channel 1.8V Specified MicroSURF™

General Description

Great Wall Semiconductor's new low cost, state of the art MicroSURF™ lateral MOSFET process technology in chipscale bondwireless packaging minimizes PCB space and $R_{DS(ON)}$ plus provides an ultra-low Qg X $R_{DS(ON)}$ figure of merit.





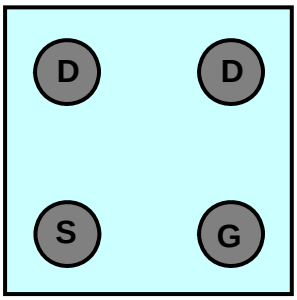
MicroSURF™ for Load Switching and PA Switch

Patent Pending

Features

- -4.9A, -12V $R_{DS(ON)}$ = 50mΩ at -4.5 Volts
- -4.4A, -12V $R_{DS(ON)}$ = 70mΩ at -2.5 Volts
- -4.0A, -12V $R_{DS(ON)}$ = 90mΩ at -1.8 Volts

- Low profile package: less than 0.8mm height when mounted on PCB.
- Occupies only 2.25 mm^2 of PCB area. Less than 25% of the area of a SSOT-6.
- Excellent thermal characteristics.



Bump Side View

Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	-12	V
V_{GSS}	Gate-Source Voltage	±8	V
I_D	Drain Current – Continuous	-4.9	A
	– Pulsed	-10	
P_D	Power Dissipation (Steady State)	1.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	ºC

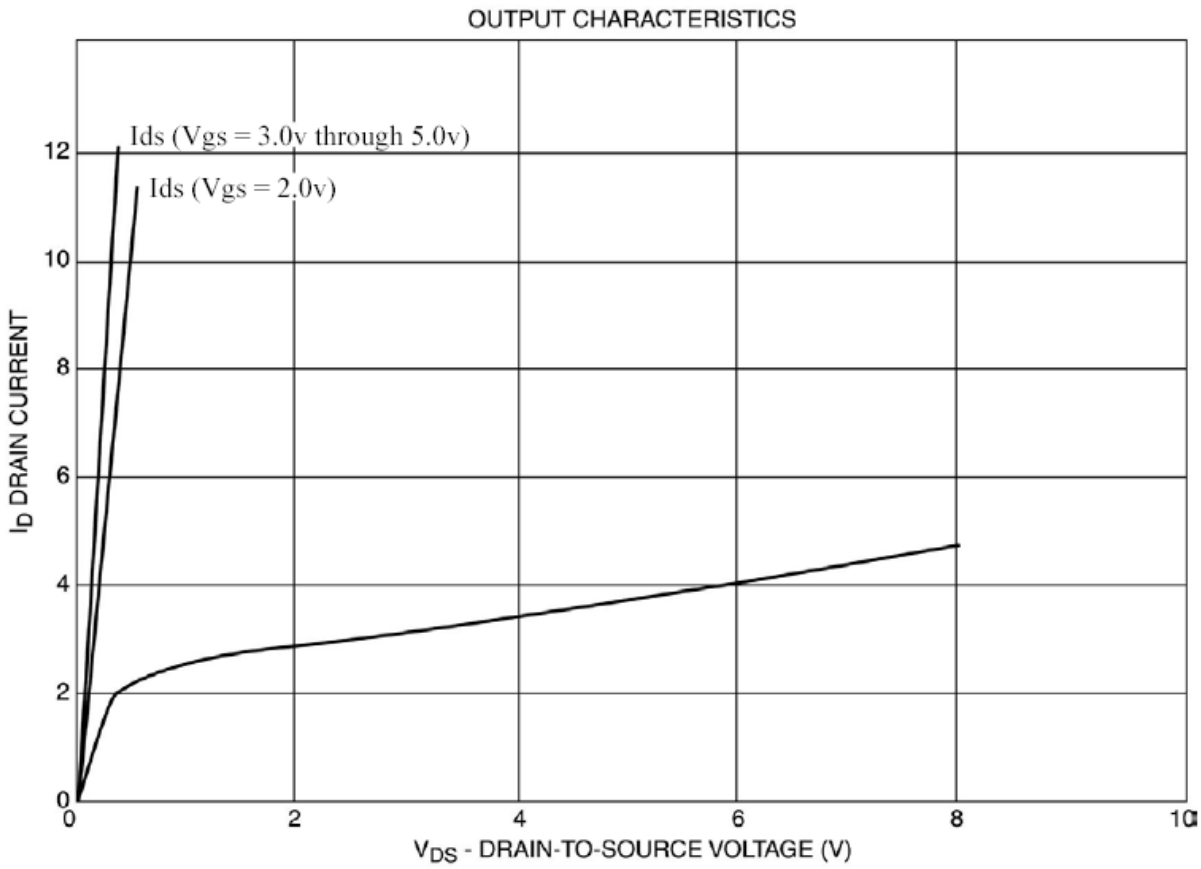
Thermal Characteristics

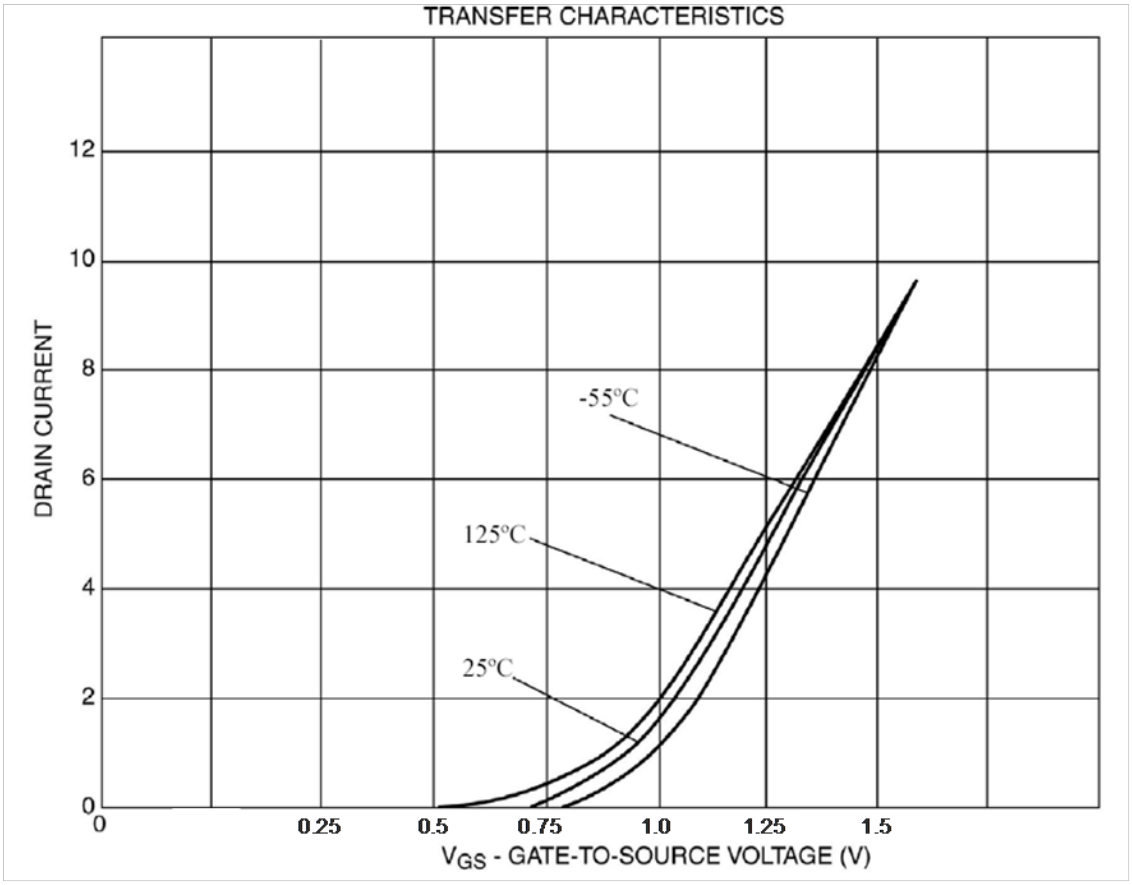
$R_{\theta JR}$	Thermal Resistance, Junction-to-Balls	12	°C/W

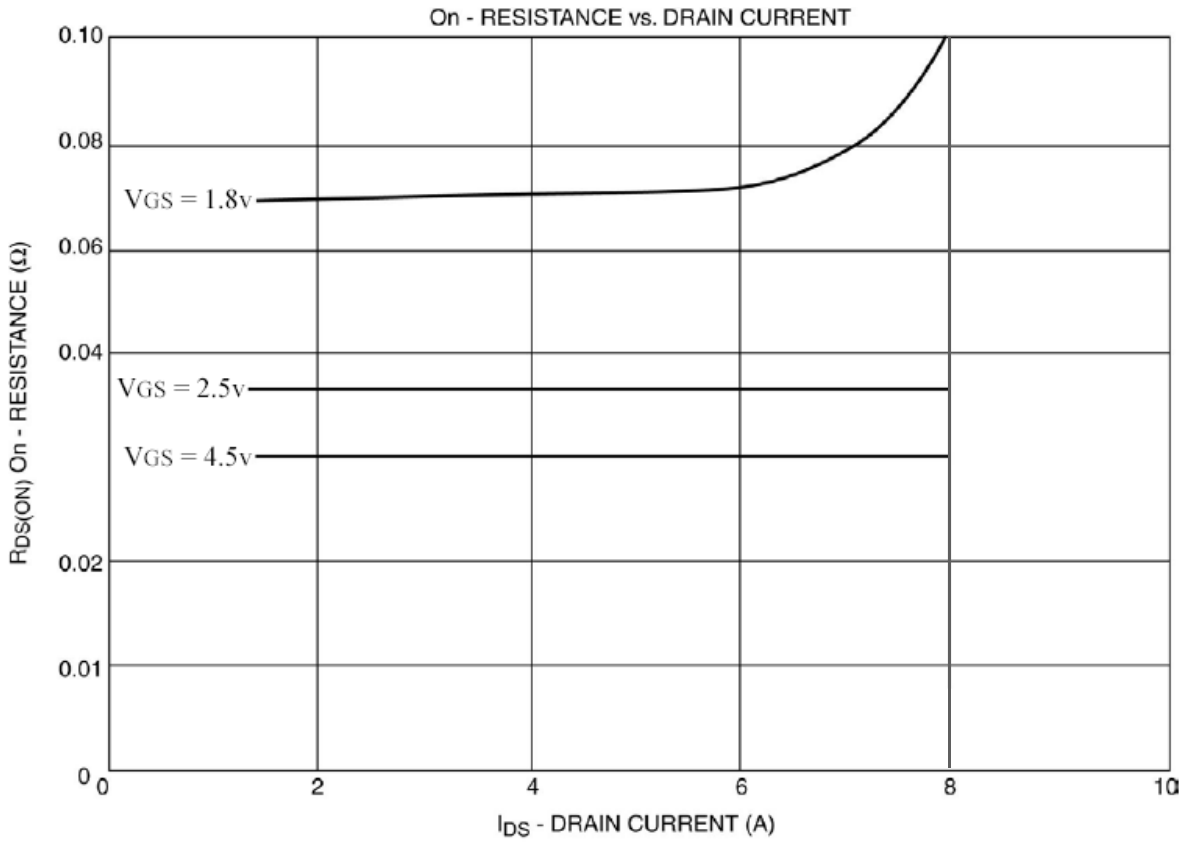
Electrical Characteristics

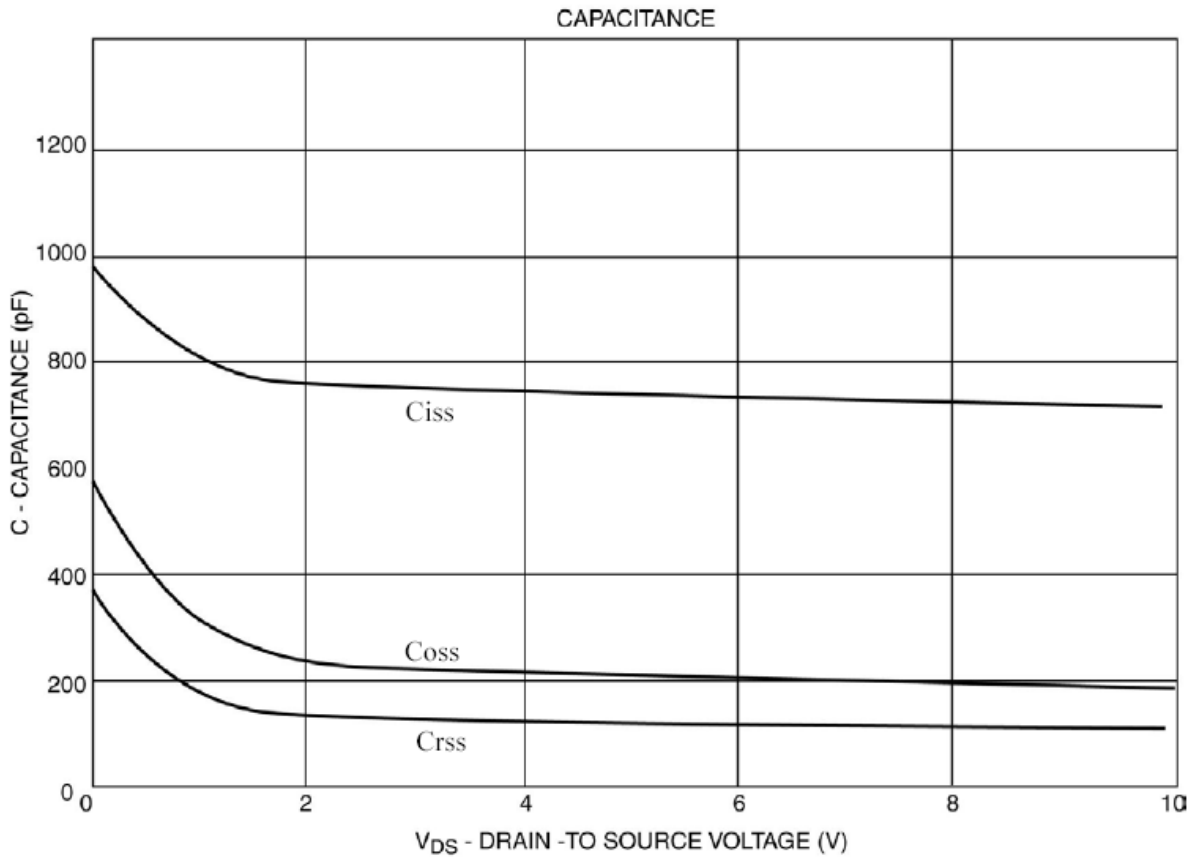
T_A=25°C unless otherwise specified

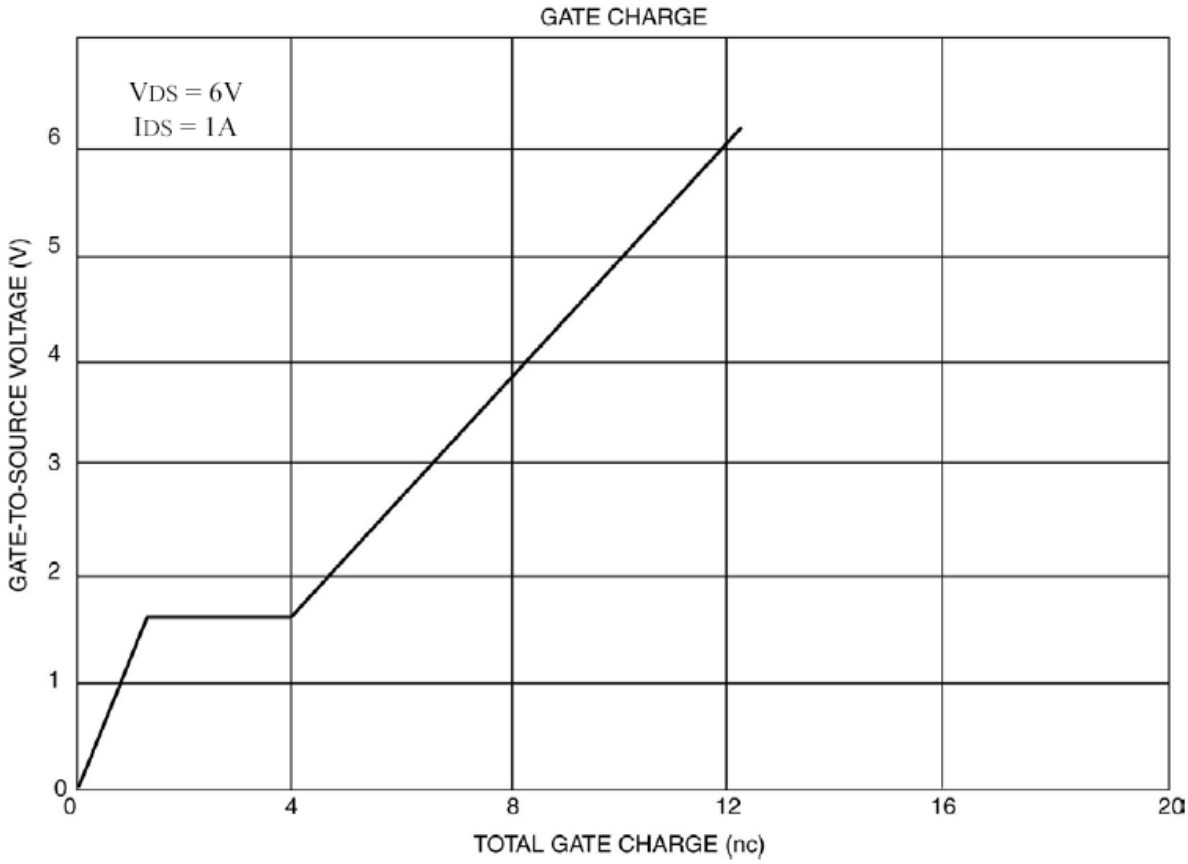
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{(BD)SS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA			-12	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-12V, V_{GS}=0V			-1	μA
	Zero Gate Voltage Drain Current	V_{DS}=-12V, V_{GS}=0V, T=70°C			-5	μA
I_{GSS}	Gate-Body Leakage	V_{GS}=±8V, V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA		-0.7		V
$r_{DS(on)}$	Drain-Source On-State Resistance	V_{GS}=-4.5V, I_D=-1A			50	mΩ
	Drain-Source On-State Resistance	V_{GS}=-2.5V, I_D=-1A			70	mΩ
	Drain-Source On-State Resistance	V_{GS}=-1.8V, I_D=-1A			90	mΩ
C_{iss}	Input Capacitance	V_{DS}=-12V, V_{GS}=0V, F=1MHZ		800		pF
C_{oss}	Output Capacitance	V_{DS}=-12V, V_{GS}=0V, F=1MHZ		250		pF
C_{rss}	Reverse Transfer Capacitance	V_{DS}=-12V, V_{GS}=0V, F=1MHZ		100		pF
Q_g	Total Gate Charge	V_{GS}=-4.5V, I_D=-1A, V_{DS}=-6V		9.0		nC
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V		-0.71		V
t_{rr}	Source-Drain Reverse Recovery Time	I_S=-1A, V_{GS}=0V, di/dt=100A/μs		40		ns

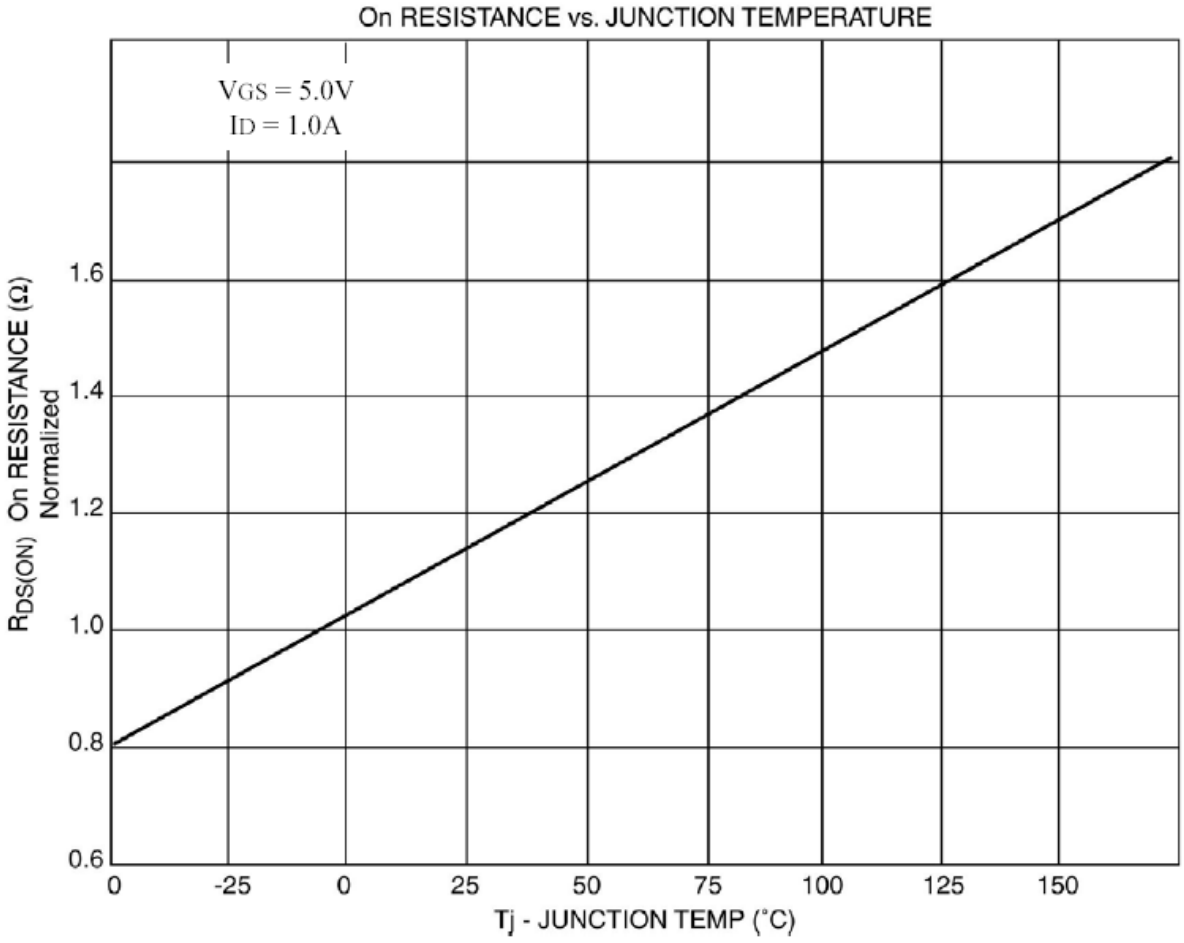

OUTPUT CHARACTERISTICS
Ids (Vgs = 3.0v through 5.0v)
Ids (Vgs = 2.0v)
ID DRAIN CURRENT
12
10
8
6
4
2
0
0
2
4
6
8
10
VDS - DRAIN-TO-SOURCE VOLTAGE (V)

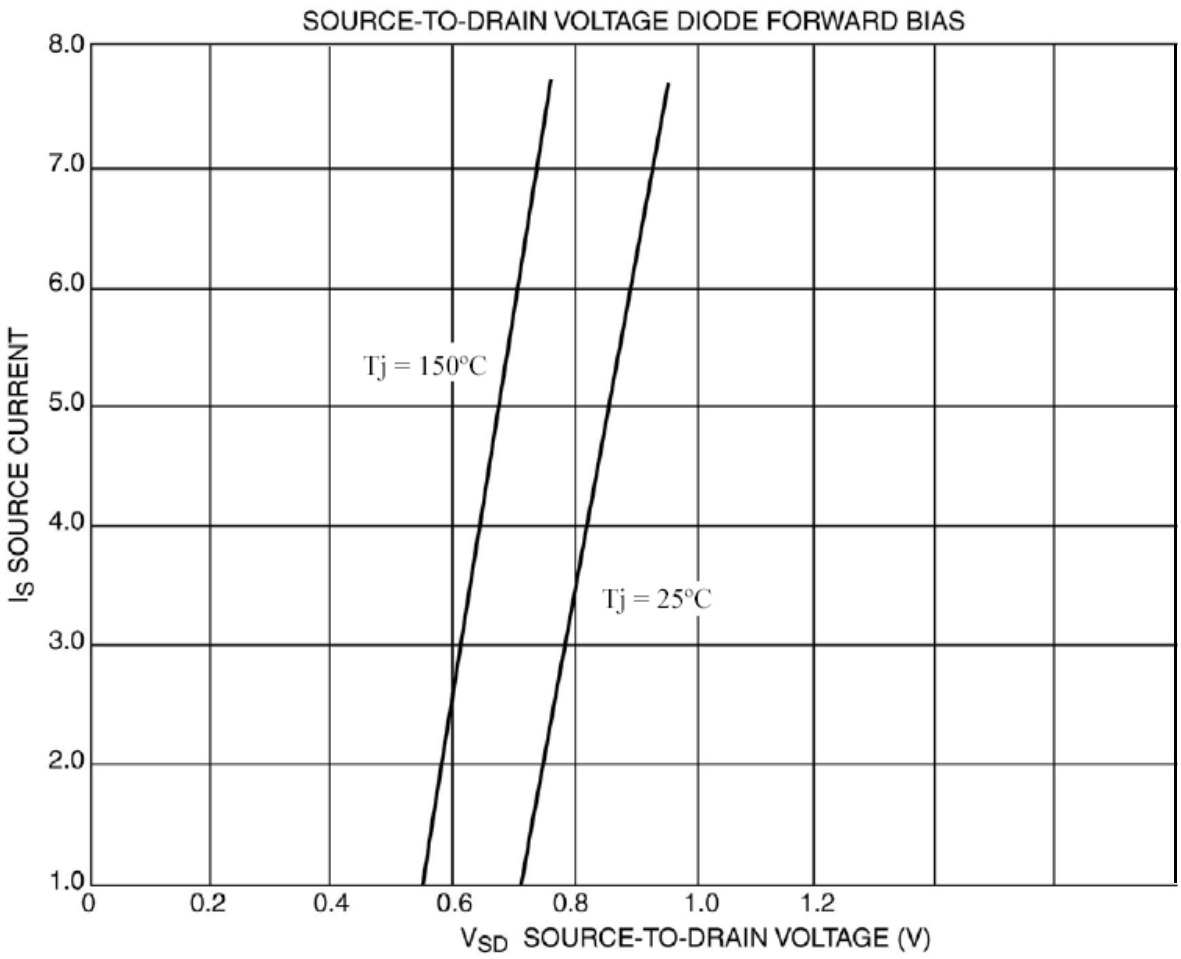

TRANSFER CHARACTERISTICS
DRAIN CURRENT
12
10
8
6
4
2
0
0
0.25
0.5
0.75
1.0
1.25
1.5
-55°C
125°C
25°C
VGS - GATE-TO-SOURCE VOLTAGE (V)

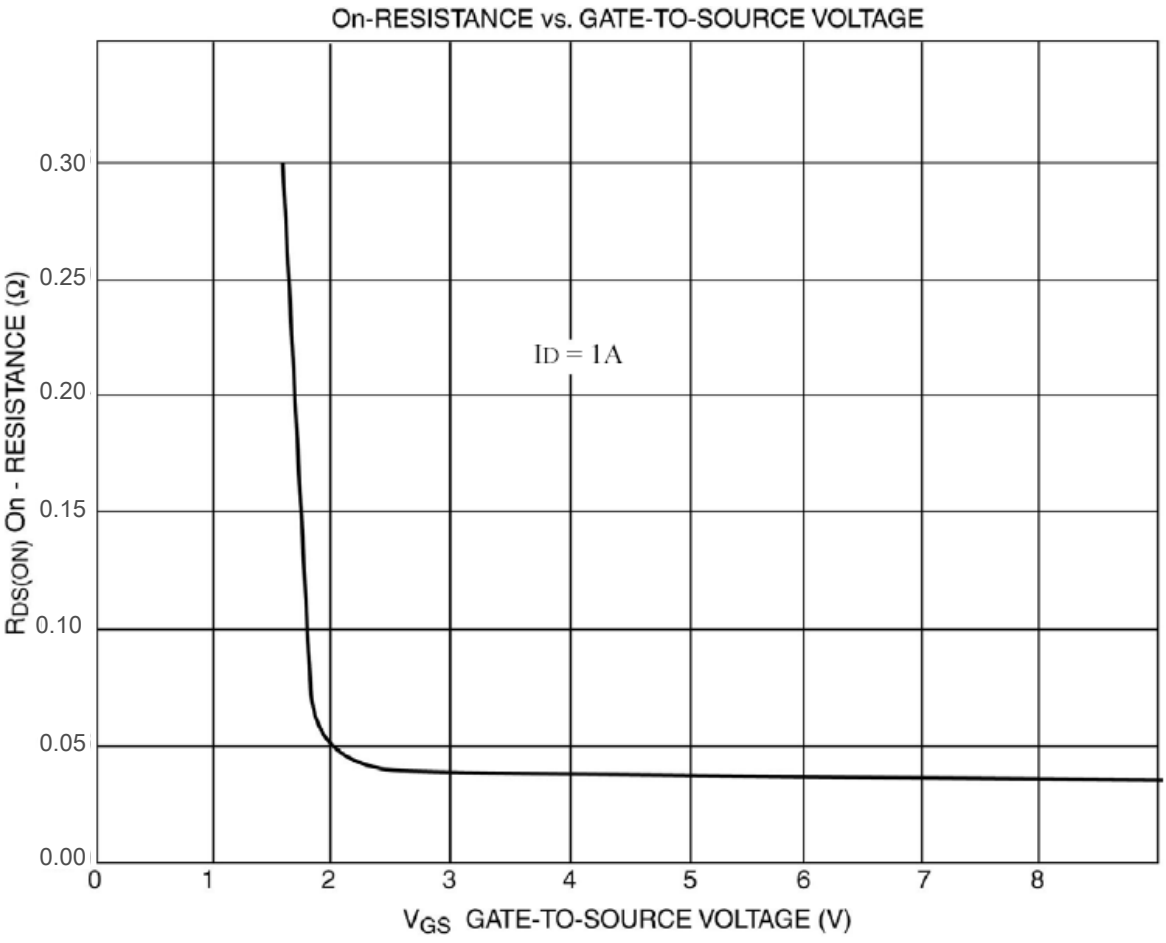

On - RESISTANCE vs. DRAIN CURRENT
0.10
0.08
0.06
0.04
0.02
0.01
0
VGS = 1.8v
VGS = 2.5v
VGS = 4.5v
RDS(ON) On - RESISTANCE (Ω)
0
2
4
6
8
10
IDS - DRAIN CURRENT (A)

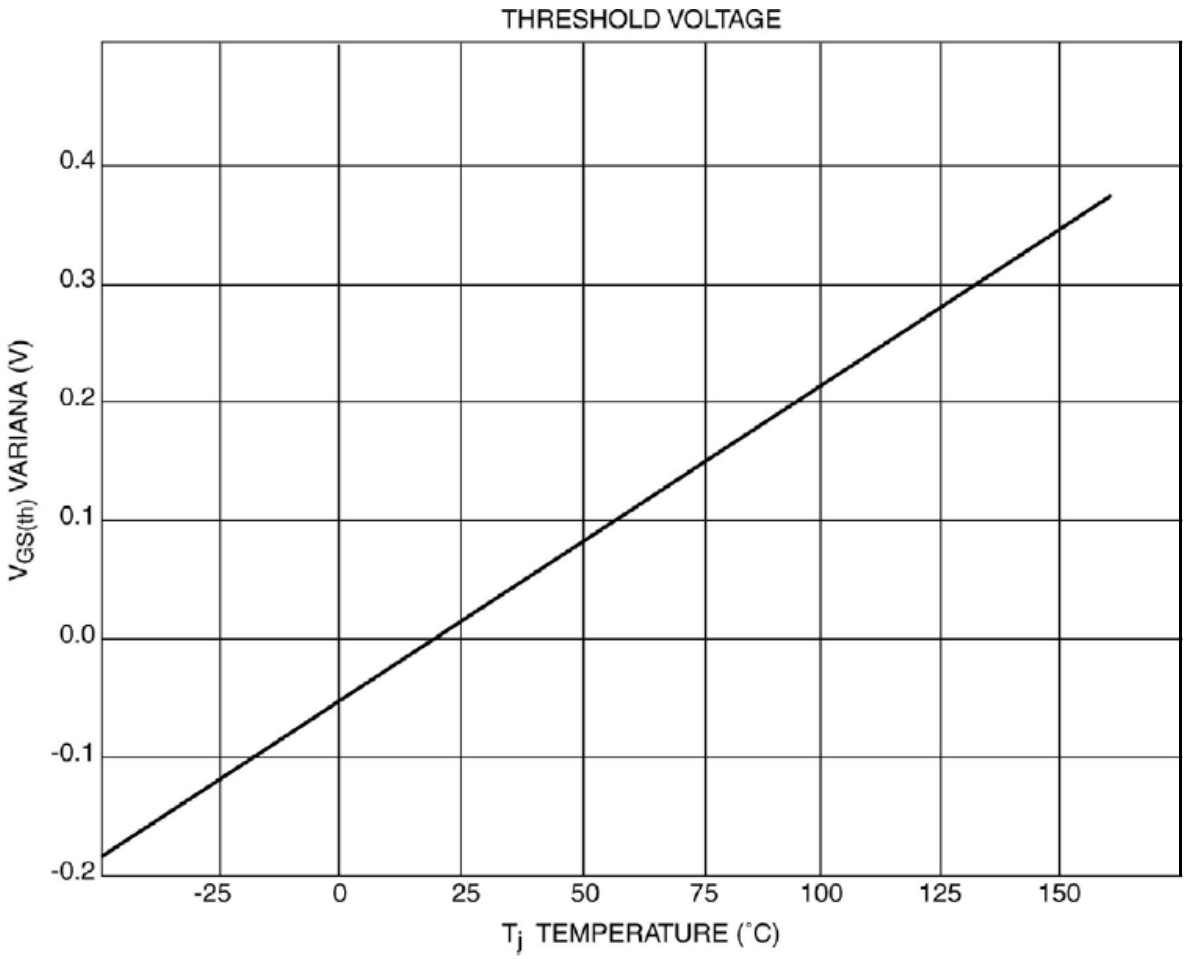

CAPACITANCE
1200
1000
800
600
400
200
0
C - CAPACITANCE (pF)
Ciss
Coss
Crss
0
2
4
6
8
10
VDS - DRAIN -TO SOURCE VOLTAGE (V)


GATE CHARGE
VDS = 6V
IDS = 1A
GATE-TO-SOURCE VOLTAGE (V)
0
1
2
3
4
5
6
0
4
8
12
16
20
TOTAL GATE CHARGE (nc)

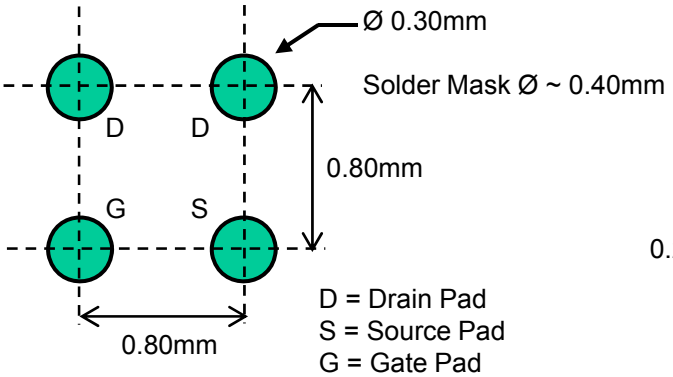

On RESISTANCE vs. JUNCTION TEMPERATURE
VGS = 5.0V
ID = 1.0A
RDS(ON) On RESISTANCE (Ω) Normalized
1.6
1.4
1.2
1.0
0.8
0.6
0
-25
0
25
50
75
100
125
150
Tj - JUNCTION TEMP (°C)


SOURCE-TO-DRAIN VOLTAGE DIODE FORWARD BIAS
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0
0.2
0.4
0.6
0.8
1.0
1.2
Tj = 150°C
Tj = 25°C
IS SOURCE CURRENT
VSD SOURCE-TO-DRAIN VOLTAGE (V)

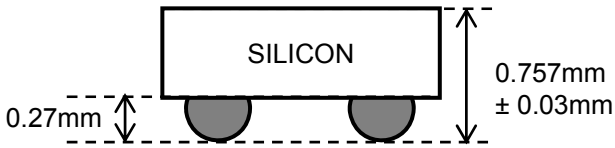

On-RESISTANCE vs. GATE-TO-SOURCE VOLTAGE
$R_{DS(ON)}$ On - RESISTANCE (Ω)
0.30
0.25
0.20
0.15
0.10
0.05
0.00
I_D = 1A
0
1
2
3
4
5
6
7
8
V_{GS} GATE-TO-SOURCE VOLTAGE (V)

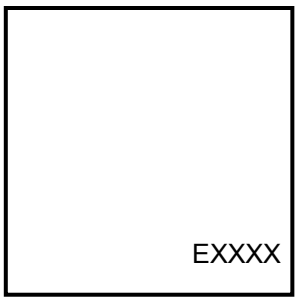

THRESHOLD VOLTAGE
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
VGS(th) VARIANA (V)
-25
0
25
50
75
100
125
150
Tj TEMPERATURE (°C)

Dimensional Outline and Pad Layout

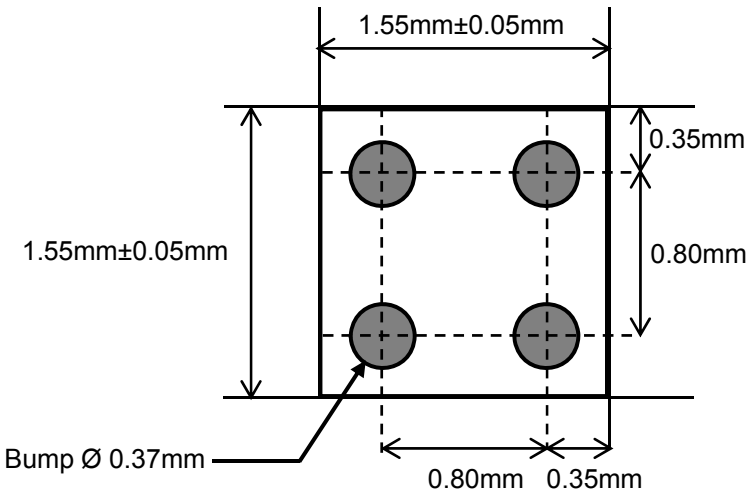


LAND PATTERN
RECOMMENDATION





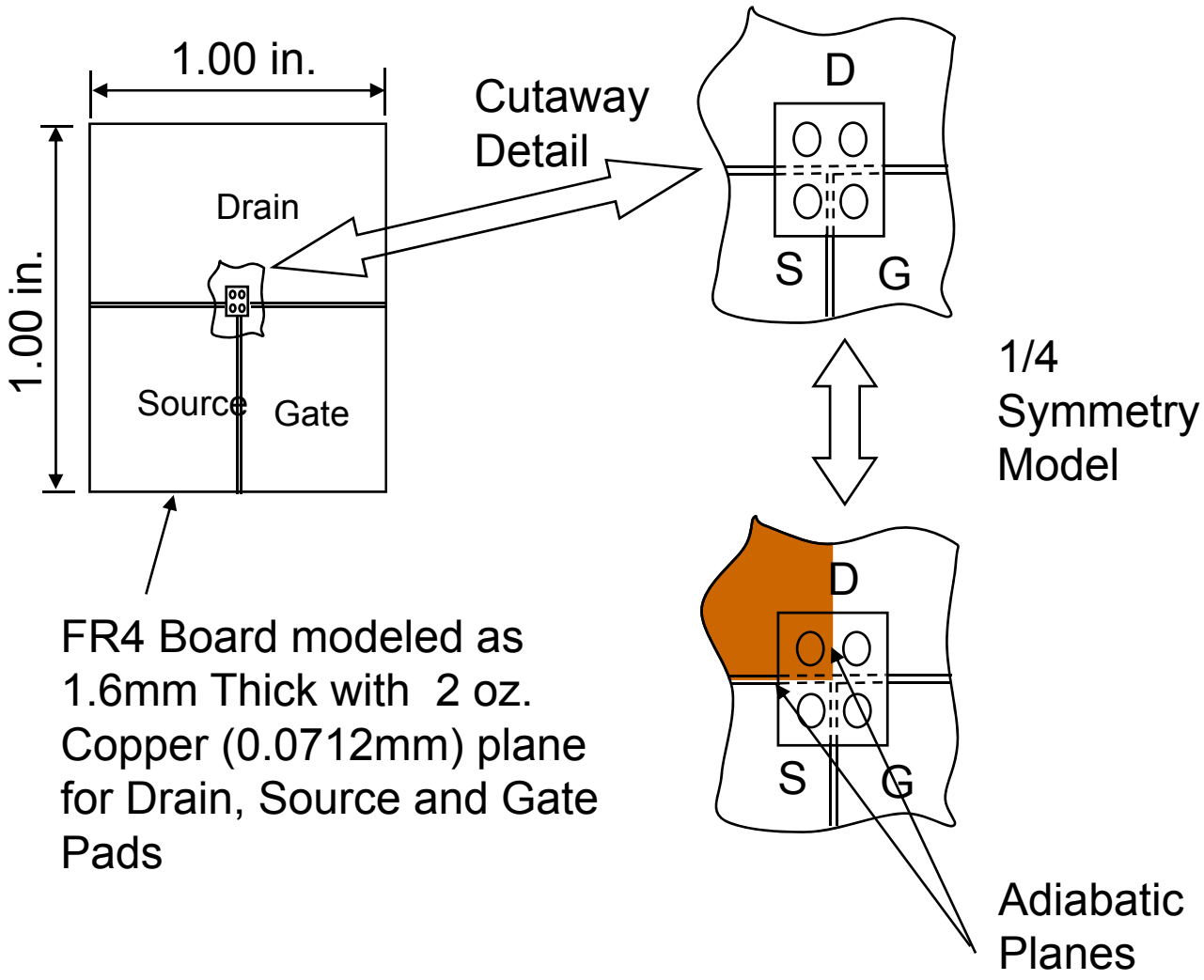
BACKSIDE VIEW (No Bump Side View)
Mark on backside of die
E = 8405P Product Code
XXXX = Date/Lot Traceability Code
Mark is located in lower right quadrant
on top of Source pad. Gate pad is located
in lower left quadrant.



Bumps are Lead Free solder 96.8 Sn / 2.6 Ag / 0.6 Cu

GWS8405P Thermal Resistance Analysis

GWS8405P Die Top View - transparent view for clarity.



FR4 Board modeled as 1.6mm Thick with 2 oz. Copper (0.0712mm) plane for Drain, Source and Gate Pads

Finite Element Model:

• Linear Thermal elements. Combination of tetrahedrals, 6 noded prisms and 8 noded bricks

• Heat Transfer conditions:
  • Bottom of FR4 board constrained to 25 degrees C
  • Power dissipation = 0.25 W per quarter model, in the form of a uniform heat flux at the die junction surface.

• Linear Thermal conduction analysis. *No convection or radiation* included in model.

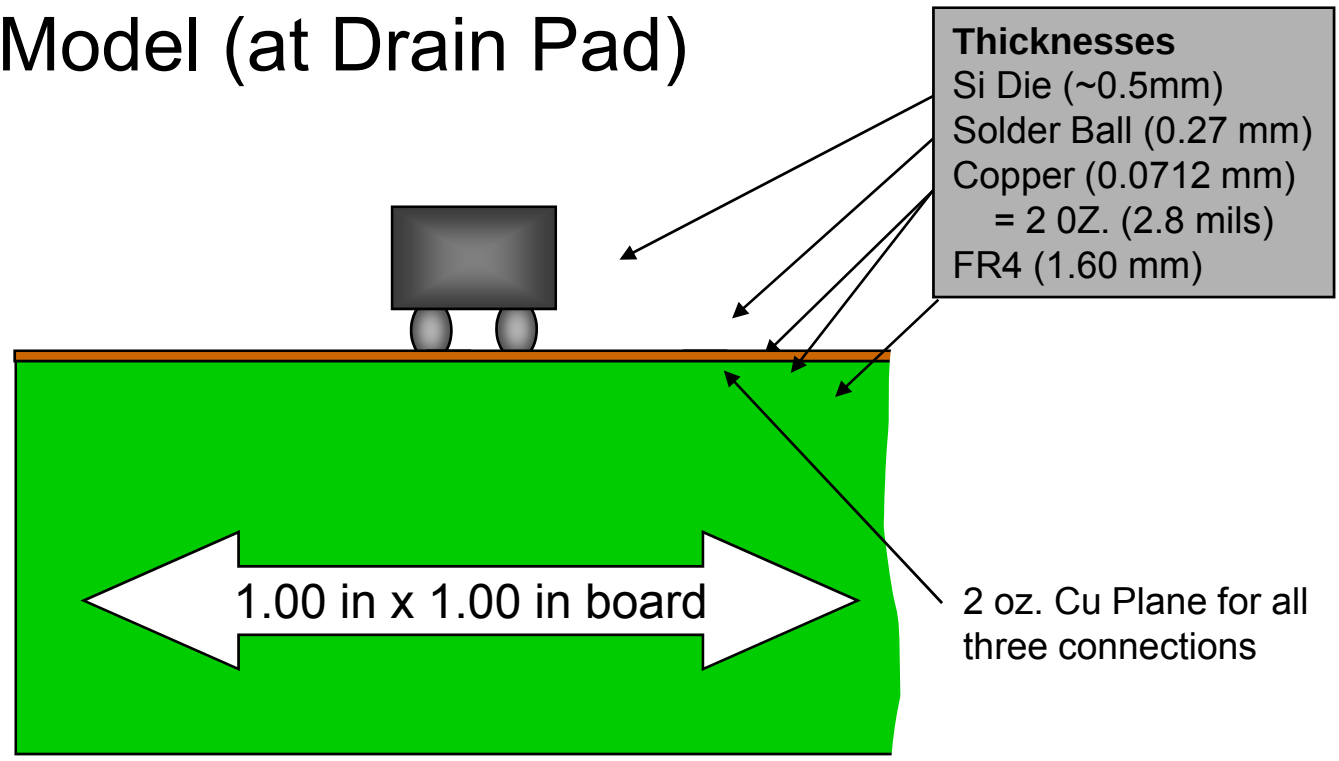
• ~4K elements.

Material Properties Used for Analysis

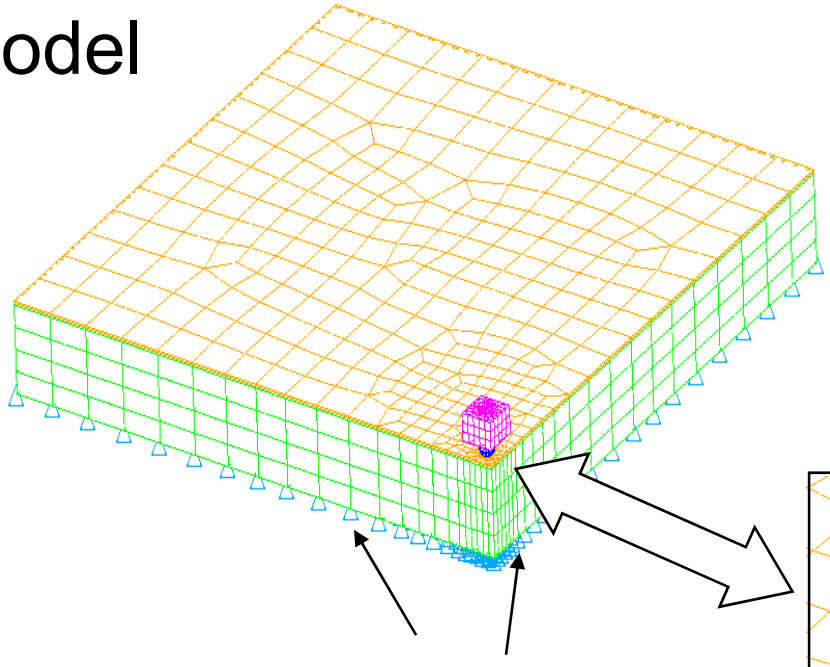
Material	Thickness (mm)	K (W/m°C)
FR4	1.60000	2.5
Copper	0.07120	390
Solder (Sn63/Pb37 eutectic)	0.27000	50
Silicon	0.50000	133
NOTE: Values obtained from http://www.boulder.nist.gov/div853/lead%20free/part2.htm		

Model: Great Wall Semiconductor GWS8405P Part

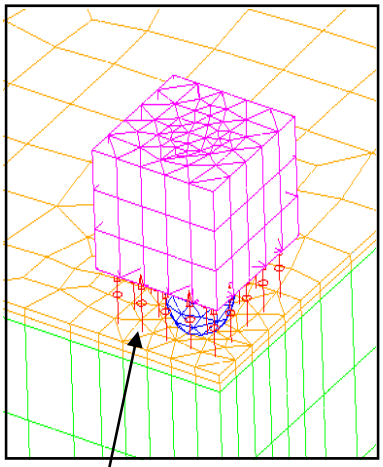
Cross Section of FEA Model (at Drain Pad)



FEA Model



Detail

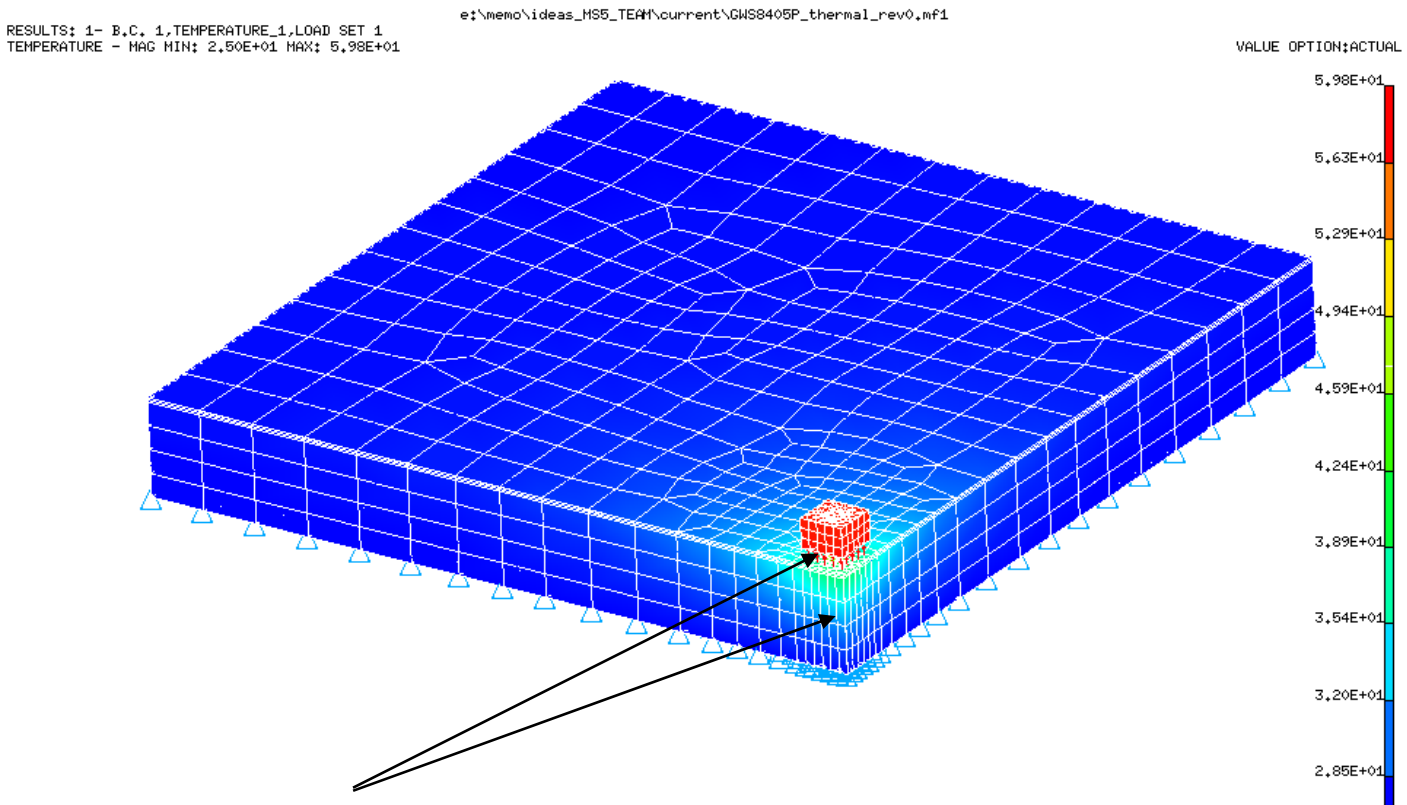


Temp Restraint

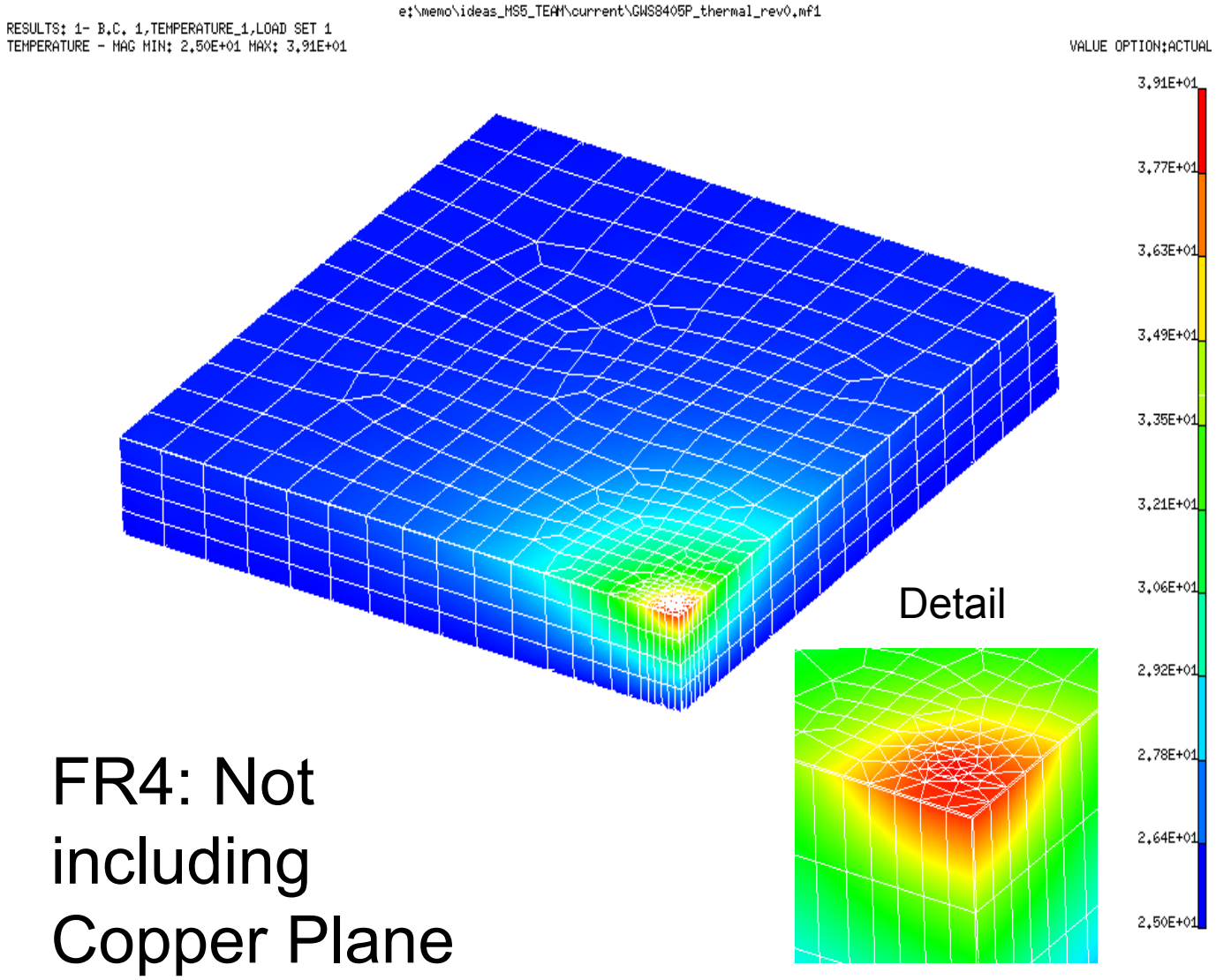
Note:
¼ symmetry used.
Solder balls use tetrahedtral elements.
All other elements are either prisms or bricks.

Heat flux
at Junction

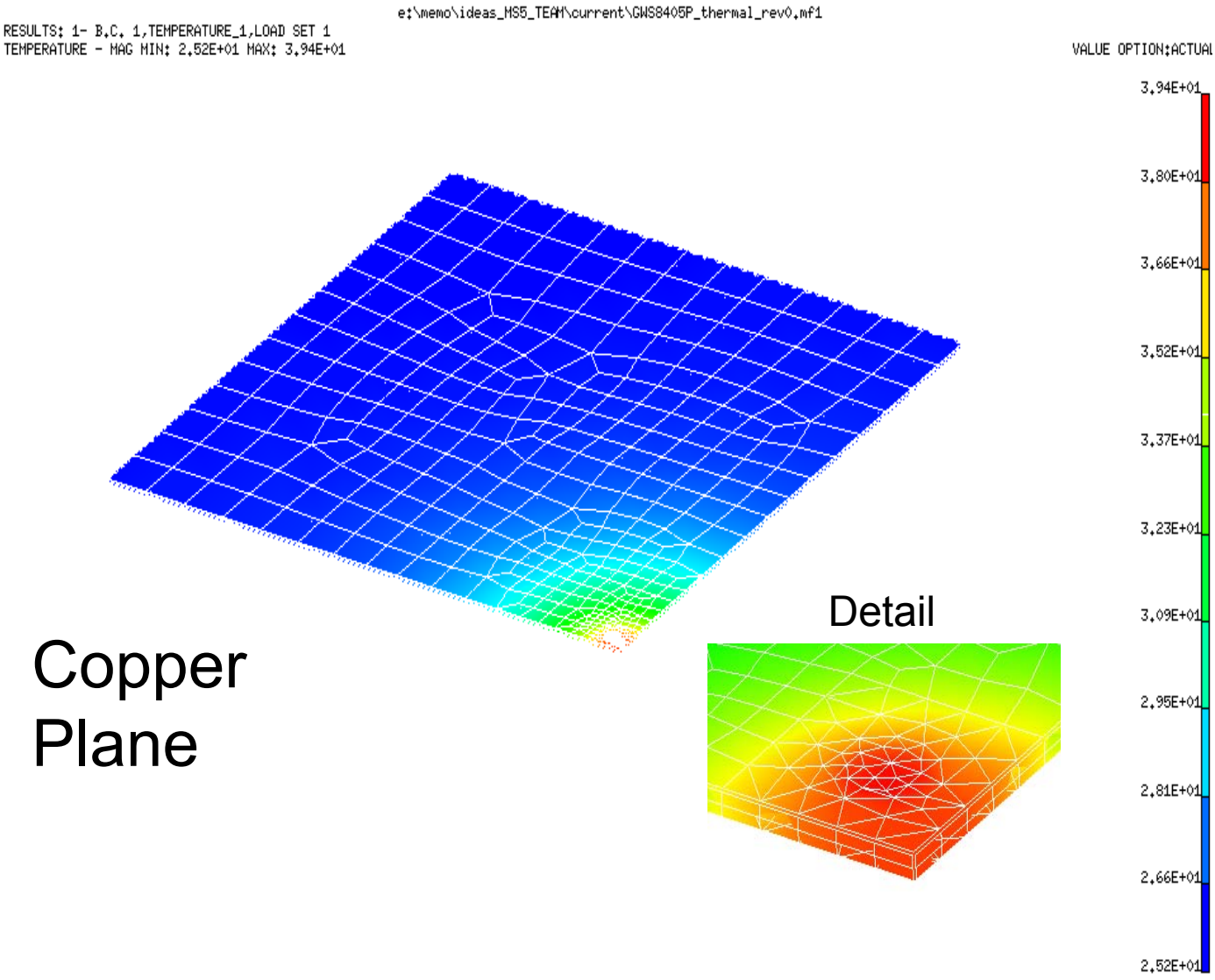
General Result:



Temperature drop is roughly 60% thru the solder ball and 40% thru the FR4 material



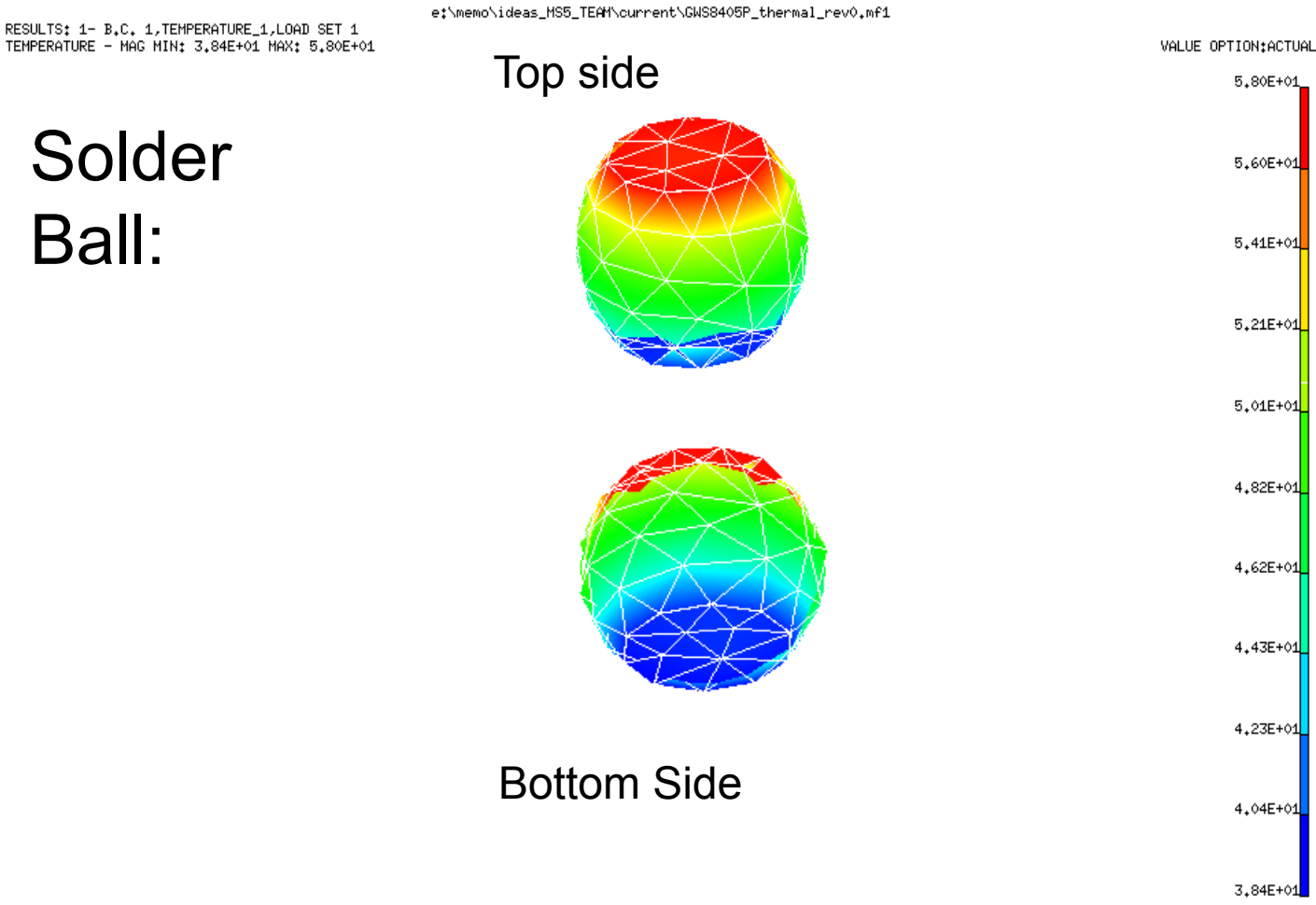
FR4: Not including Copper Plane



Copper Plane

Detail

Solder Ball:


e:\memo\ideas_MS5_TEAM\current\GWS8405P_thermal_rev0.mf1
RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 3.84E+01 MAX: 5.80E+01
VALUE OPTION:ACTUAL
5.80E+01
5.60E+01
5.41E+01
5.21E+01
5.01E+01
4.82E+01
4.62E+01
4.43E+01
4.23E+01
4.04E+01
3.84E+01
Top side
Bottom Side

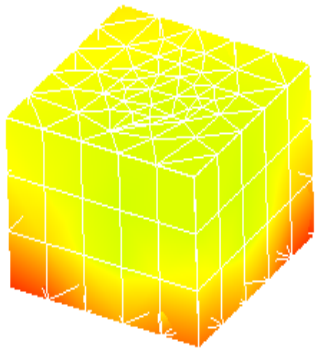
e:\memo\ideas_MS5_TEAM\current\GWS8405P_thermal_rev0.mf1

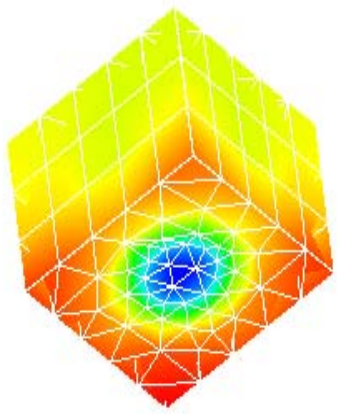
RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 5.74E+01 MAX: 5.98E+01

VALUE OPTION:ACTUAL

Silicon:

Top Side





NOTE: The difference between min and max temperatures is only 2.5°C.

Bottom Side

Summary of Results

Thermal Resistance calculations:

$$\theta = \frac{\Delta T}{\text{Power}}$$

Layer *	ΔT (°C)	Resistance (°C/W)
Junction to bottom of Ball (all four balls)	12.0000	12.0000
Ball to bottom of Copper Plane	0.0030	0.0030
Copper Plane to bottom of FR4	13.6300	13.6300
Total Junction to bottom of FR4	**25.6330**	**25.6330**
* temperatures are taken on the hottest spot in each layer and the node directly underneath it on the opposite side