



GWS6N60 for Soft Switching

Features

- Low RDS (on)
- Ultra low gate charge and figure of merit
- Patent Pending Lateral Power™ technology for High Frequency Switching
- Low Thermal Resistance Chip-Scale package
Occupies 1/3rd the area of S08

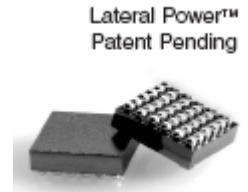
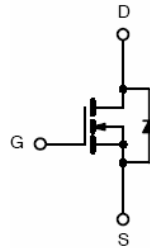
Applications

- DC/DC Converters
- Portable Equipment
- OR'ing Diodes

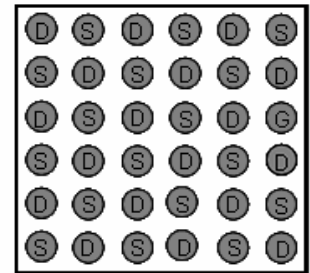
Description

The GWS6N60 is a 60V, 17mΩ, chip-scale, N-Channel lateral MOSFET. The device uses Great Wall Semiconductor's patented Lateral Power™ technology that uniquely integrates low cost CMOS and wafer bumping fabrication processes. The MicroSurf™ chipscale package offers small size, low profile, and is fully compatible with standard SMT assembly processes. The GWS6N60 device offers unprecedented low on resistance and total gate charge, outperforming conventional trench MOSFETs and enabling high frequency, high efficiency synchronous rectification or low voltage switching. The device offers extremely high power density, reducing the board size of DC-DC converters and other power management systems.

Product Summary			
I_D	$T_A=25^\circ\text{C}$	6A	Max
$V_{(BR)DSS}$	$I_D=1\text{mA}$	60V	Max
$r_{DS(on)}$	$V_{GS}=8\text{V}$	17 mΩ	Typ
Q_g	$V_{GS}=8\text{V}$	12nC	Typ



Patent Pending



Bottom: Bump Side

Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	+/- 15	
Drain Current	- Continuous	I_D	A
	- Pulsed	I_{DM}	
Single Pulse Avalanche Current	$T_{av} < 11\mu\text{s}$	I_{AS}	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	W
	$T_A=70^\circ\text{C}$		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Thermal Resistance ^a	- Junction-to-Ambient	R_{thJA}	$^\circ\text{C/W}$
	- Junction-to-Ball	R_{thJB}	

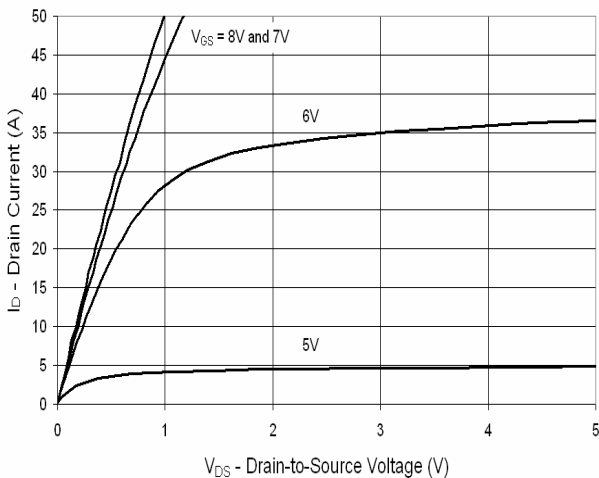
^a When mounted on 1 inch square 2oz copper clad FR-4

Electrical Characteristics

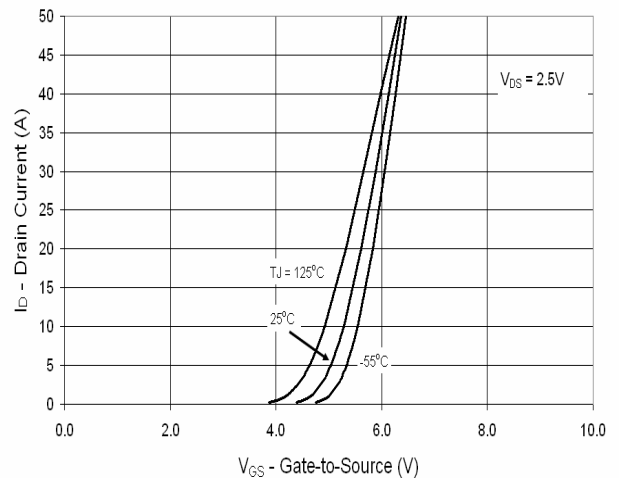
$T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			10	μA
I_{GSS}	Gate-Body Leakage	$V_{GS}=12V, V_{DS}=0V$			150	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.6		3.8	V
$r_{DS(on)}$	Drain-to-Source On-State Resistance	$V_{GS}=8V, I_D=6A$		17	20	m Ω
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1MHz$		860		pF
C_{oss}	Output Capacitance			480		pF
C_{rss}	Reverse Transfer Capacitance			27		pF
Q_g	Total Gate Charge	$V_{GS}=8V, I_D=6A, V_{DS}=48V$		12	15	nC
Q_{gs}	Gate-to-Source Charge			4		nC
Q_{gd}	Gate-to-Drain Charge			4		nC
t_{rr}	Source-to-Drain Reverse Recovery Time	$I_S=4A, di/dt=33A/\mu S$		150		nS
V_{SD}	Diode Forward Voltage	$I_S=4A, V_{GS}=0V$		0.75	1.0	V

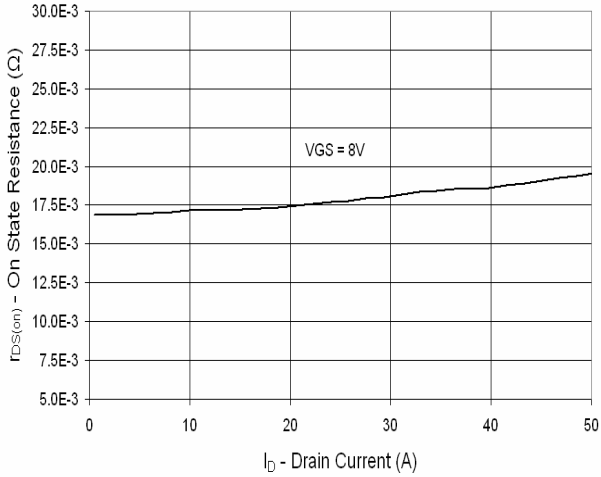
Output Characteristics



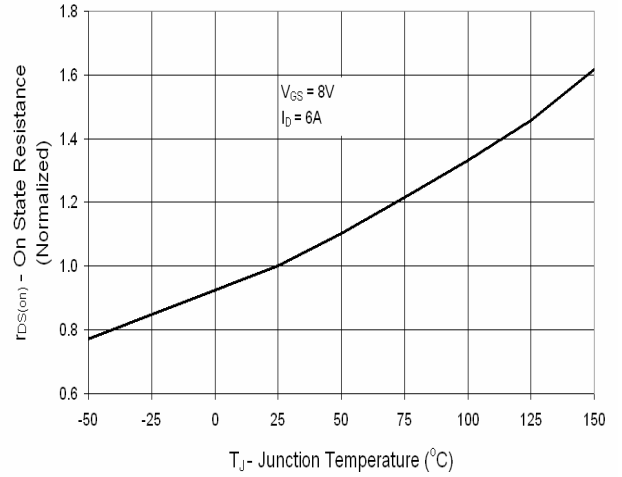
Transfer Characteristics



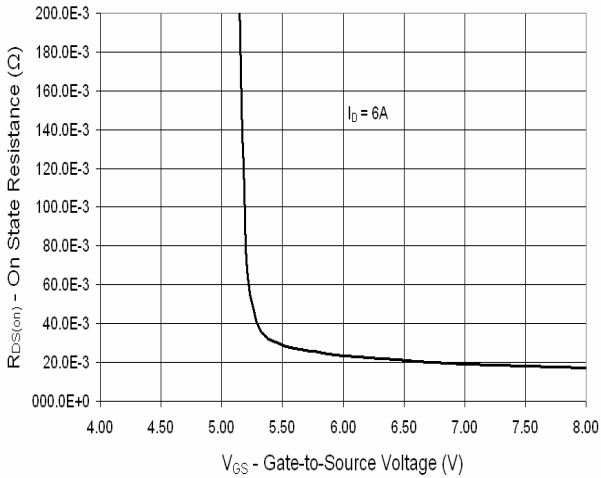
On Resistance vs. Drain Current



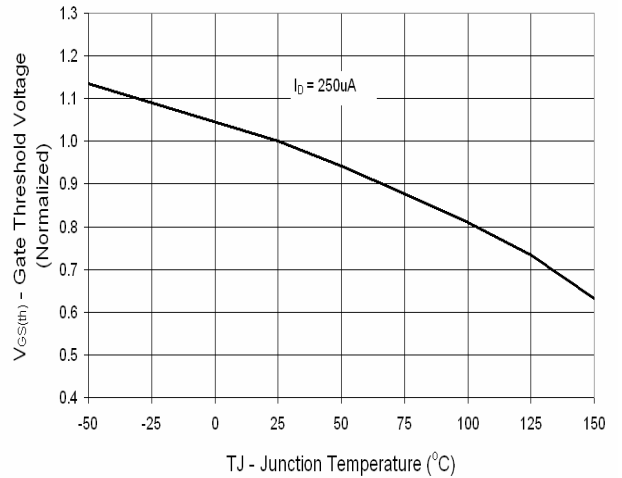
On State Resistance vs. Junction Temperature



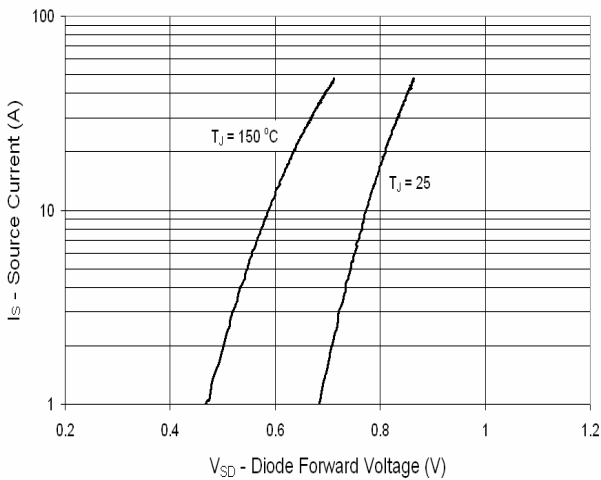
On-Resistance vs. Gate-to-Source Voltage



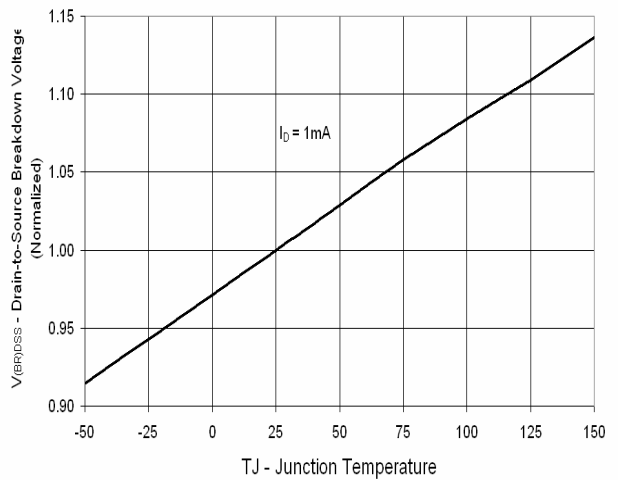
Gate Threshold Voltage vs. Junction Temperature



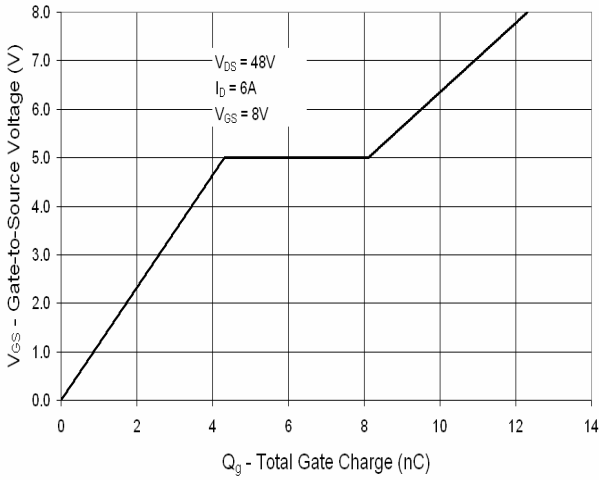
Source-Drain Diode Forward Voltage



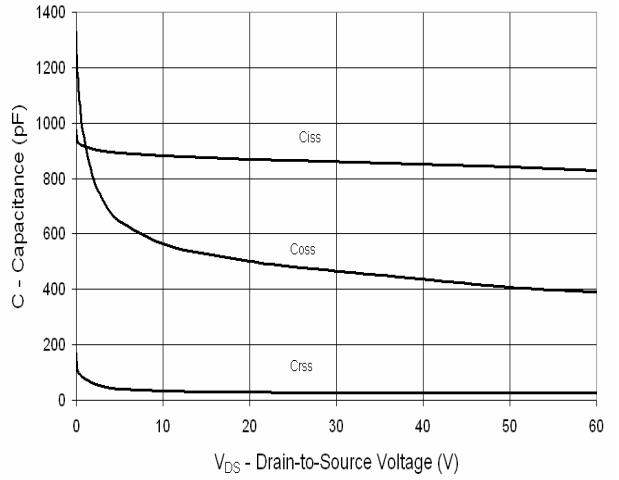
Drain-to-Source Breakdown Voltage vs. TJ



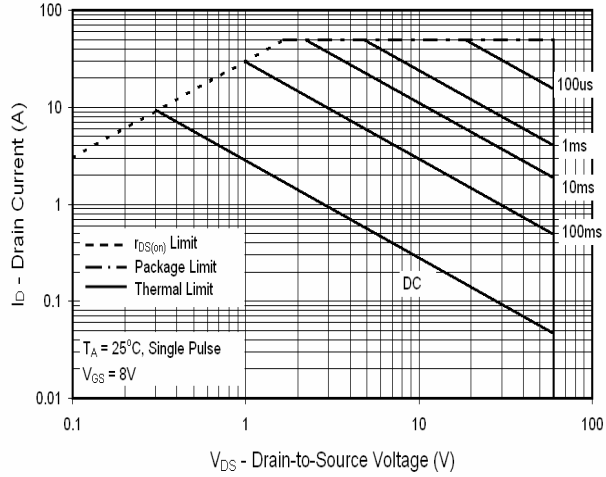
Gate Charge



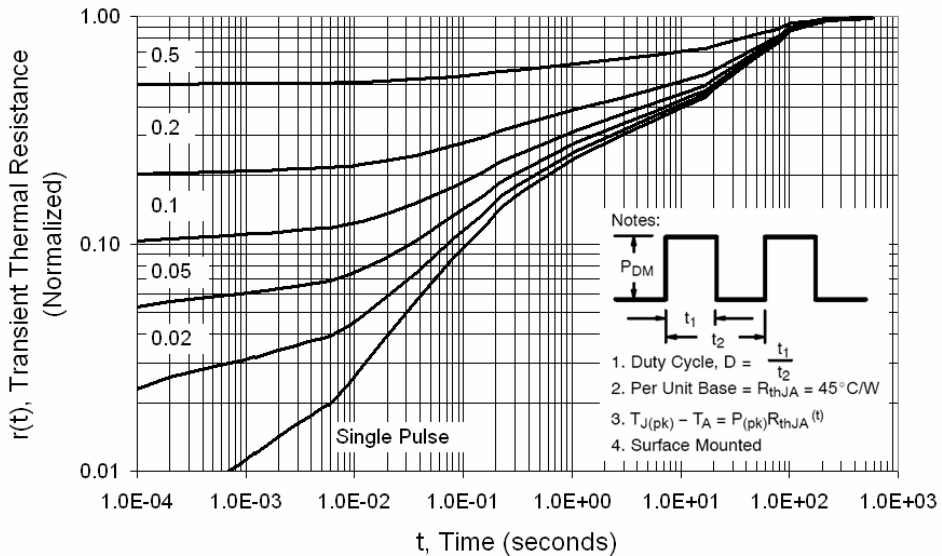
Capacitance



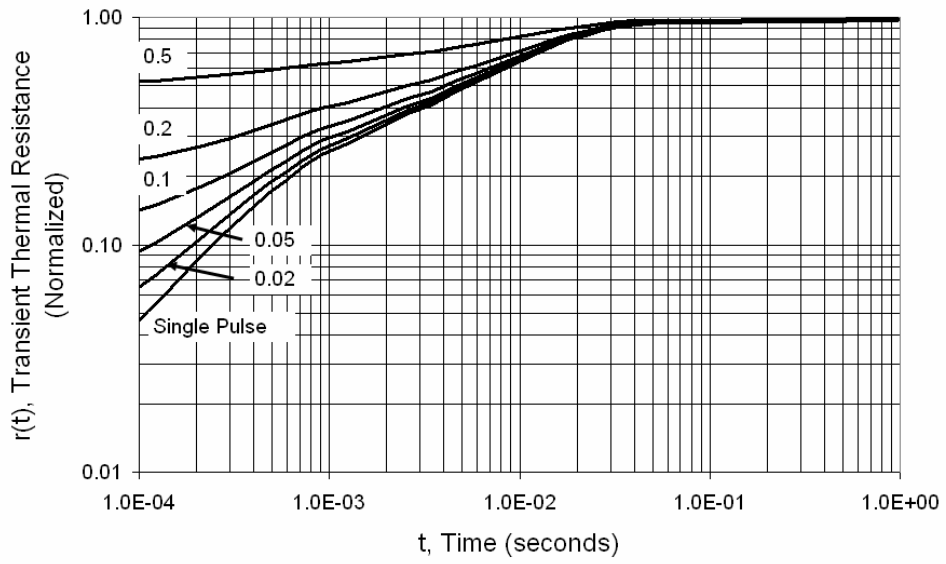
Maximum Rated Forward Biased Safe Operating Area



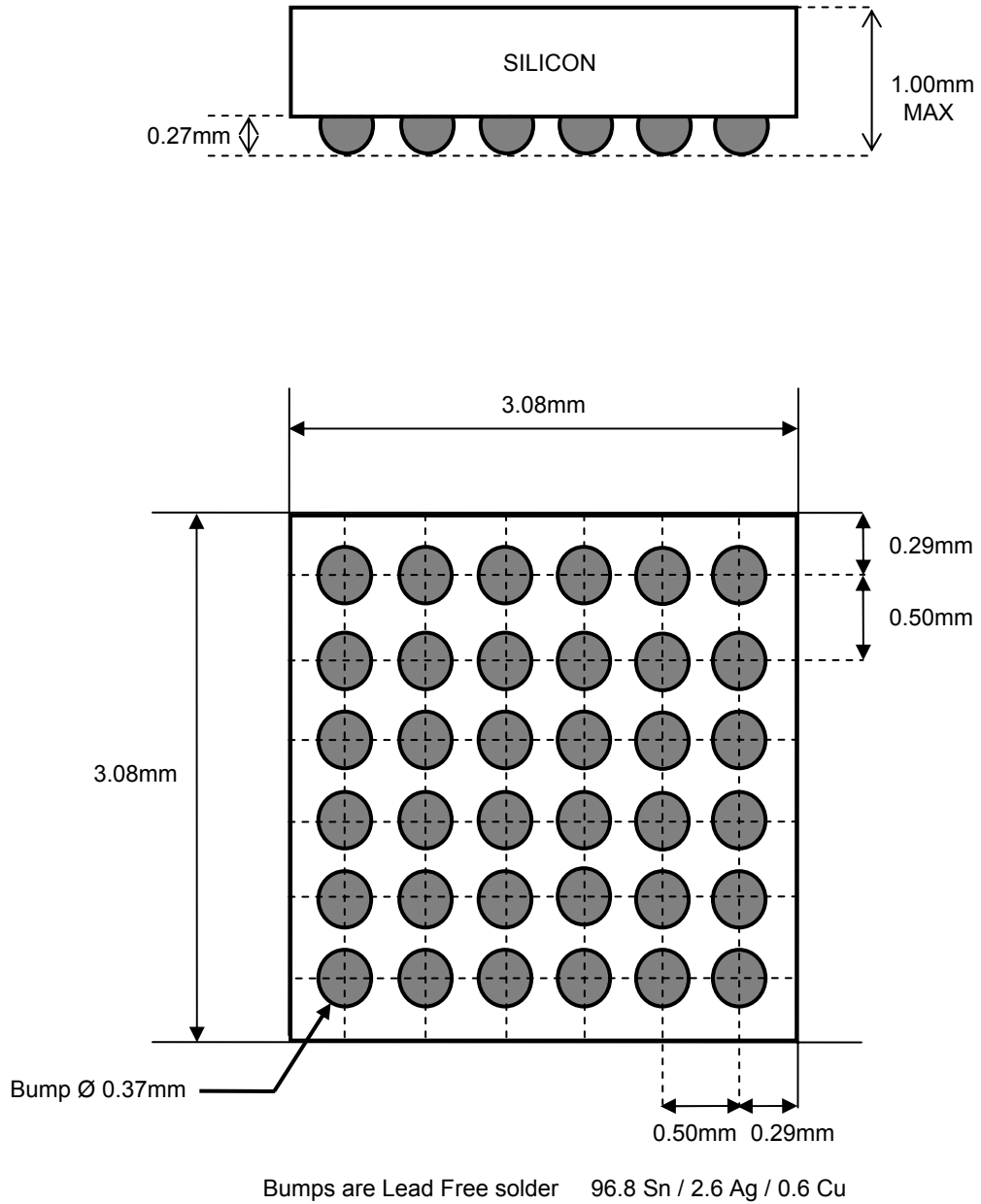
Transient Thermal Response, Junction-to-Ambient



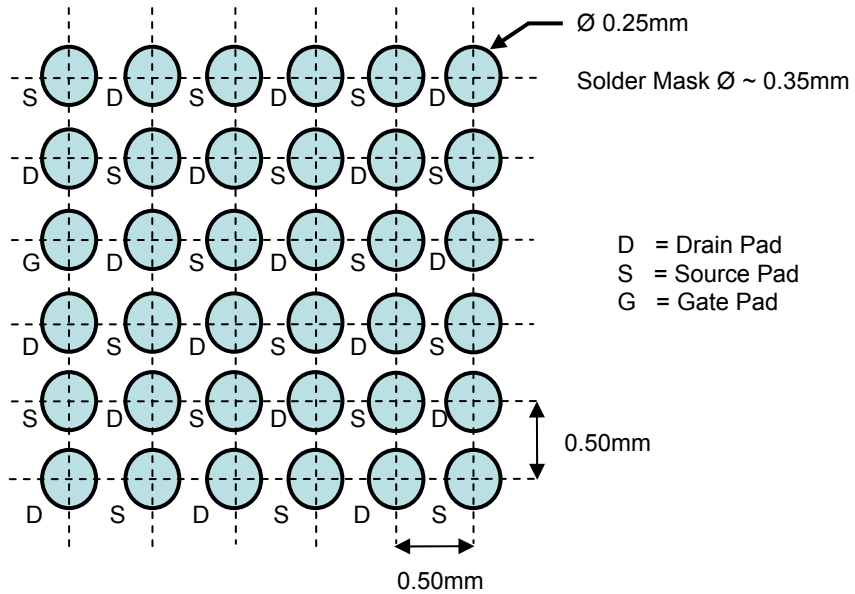
Transient Thermal Response, Junction-to-Ball



Dimensional Outline and Pad Layout



Dimensional Outline and Pad Layout



LAND PATTERN RECOMMENDATION



MARK ON BACKSIDE OF DIE

J = GWS6N60 Product Code

XXXX = Date/Lot Traceability Code