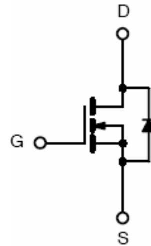
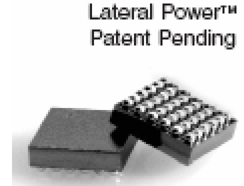
GWS5N100 for Soft Switching

Product Summary			
I_D	T_A=25°C	5A	Max
$V_{(BR)DSS}$	I_D=250uA	100V	Max
$r_{DS(on)}$	V_{GS}=8V	43 mΩ	Typ
Q_g	V_{GS}=8V	9nC	Typ

Features

- Low RDS (on)
- Ultra low gate charge and figure of merit
- Patent Pending Lateral PowerTM technology for High Frequency Switching
- Low Thermal Resistance Chip-Scale package Occupies 1/3rd the area of S08





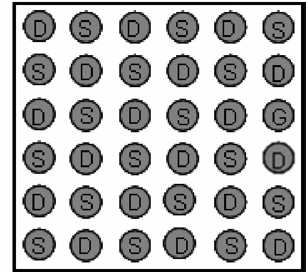
Applications

- DC/DC Converters
- Telecom/Server
- Industrial and Automotive

Description

The GWS5N100 is a 100V, 43mΩ, chip-scale, N-Channel lateral MOSFET The device uses Great Wall Semiconductor's patented Lateral Power^{TM} technology that uniquely integrates low cost CMOS and wafer bumping fabrication processes. The MicroSurf^{TM} chipscale package offers small size, low profile, and is fully compatible with standard SMT assembly processes. The GWS5N100 device offers unprecedented low on resistance and total gate charge, outperforming conventional trench MOSFETs and enabling high frequency, high efficiency synchronous rectification or low to medium voltage switching. The device offers extremely high power density, reducing the board size of DC-DC converters and other power management systems.

Patent Pending



Bottom: Bump Side

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-Source Voltage			V_{DS}	100	V
Gate-Source Voltage			V_{GS}	+/- 15	
Drain Current	- Continuous		I_D	5	A
	- Pulsed (10uS pulse width)		I_{DM}	50	
Single Pulse Avalanche Current[b]		Tav < 4uS	I_{AS}	10	A
Maximum Power Dissipation		T_A=25°C	P_D	2.8	W
		T_A=70°C		1.8	
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to 150	°C
Thermal Resistance[a]	- Junction-to-Ambient		R_{thJA}	45.0	°C/W
	- Junction-to-Ball		R_{thJB}	2.0	

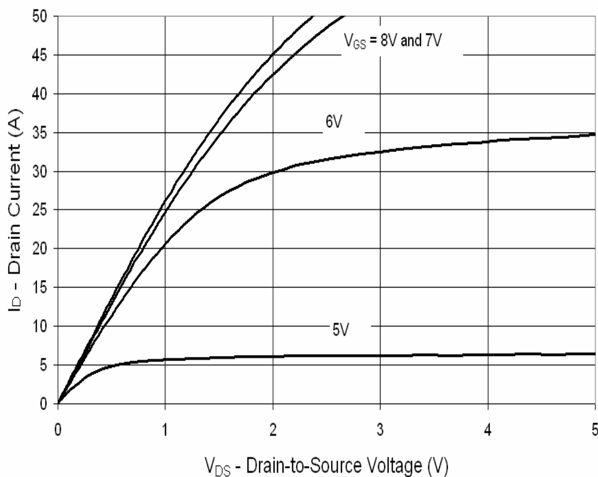
[a] When mounted on 1 inch square 2oz copper clad FR-4

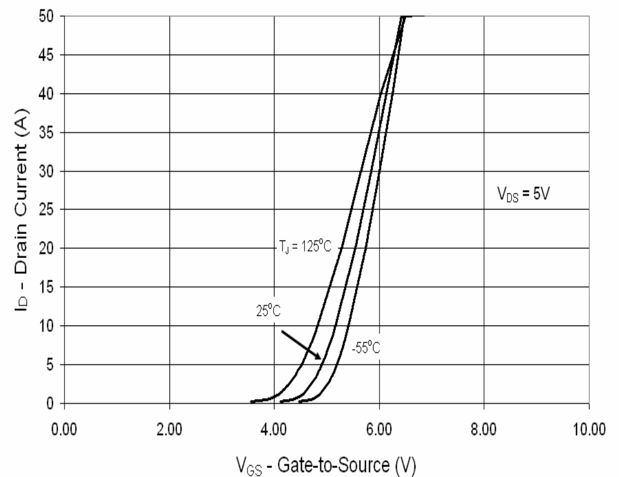
[b] Preliminary Data Sheet - Specifications subject to change.

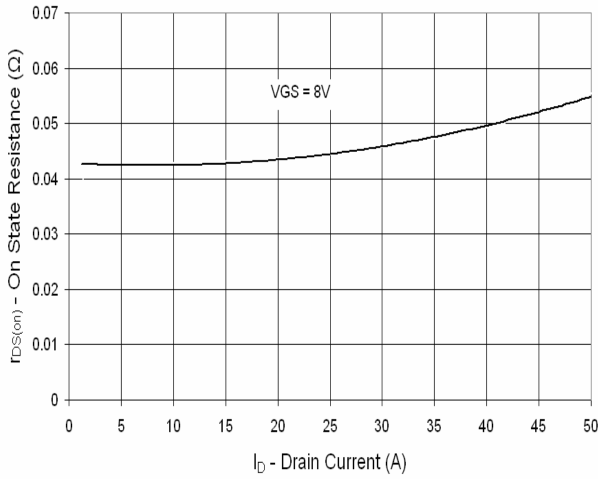
Electrical Characteristics

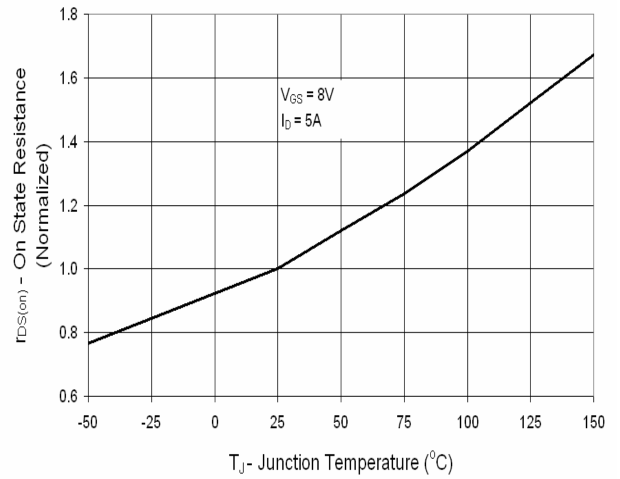
T_J=25°C unless otherwise specified

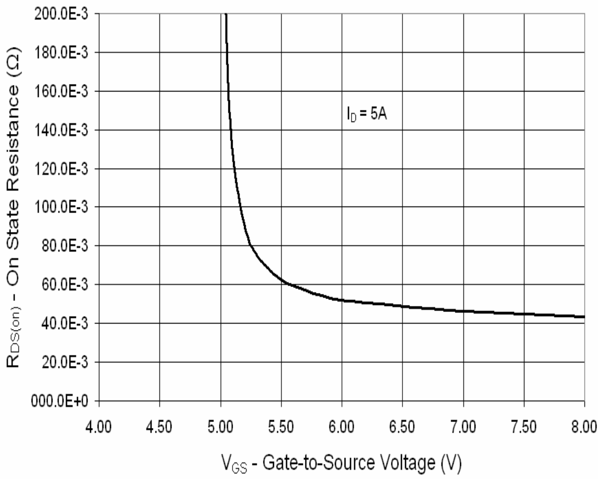
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=90V, V_{GS}=0V			10	μA
I_{GSS}	Gate-Body Leakage	V_{GS}=12V, V_{DS}=0V			150	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2.6		3.8	V
$r_{DS(on)}$	Drain-to-Source On-State Resistance	V_{GS}=8V, I_D=6A		43	55	mΩ
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MH_Z		580		pF
C_{oss}	Output Capacitance			350		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
Q_g	Total Gate Charge	V_{GS}=8V, I_D=6A, V_{DS}=48V		9	14	nC
Q_{gs}	Gate-to-Source Charge			3		nC
Q_{gd}	Gate-to-Drain Charge			3		nC
t_{rr}	Source-to-Drain Reverse Recovery Time	I_S=4A, di/dt=33A/uS		150		nS
V_{SD}	Diode Forward Voltage	I_S=4A, V_{GS}=0V		0.75	1.0	V

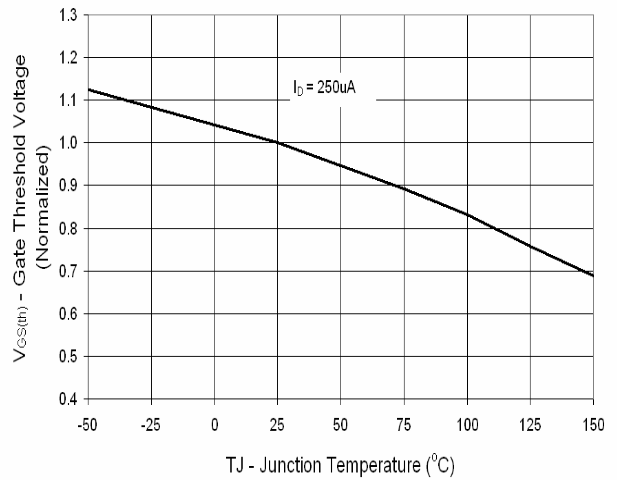


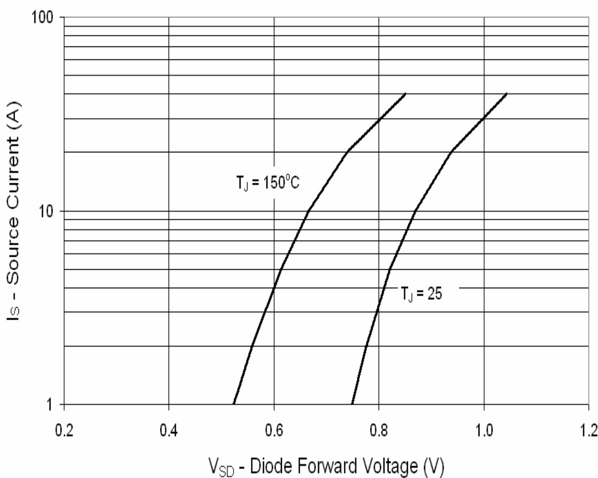


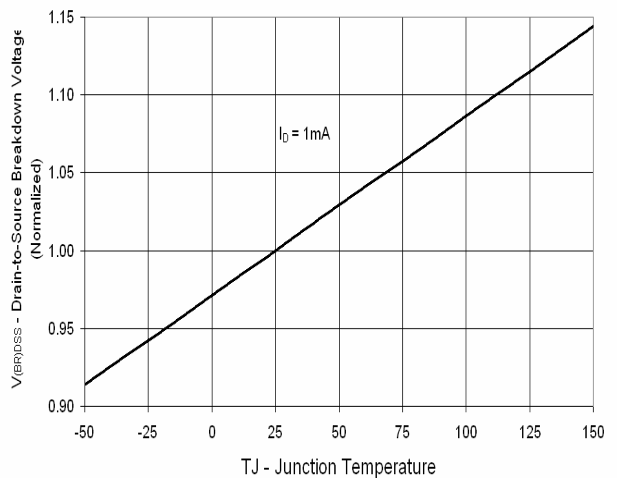

On Resistance vs. Drain Current
VGS = 8V
rDS(on) - On State Resistance (Ω)
ID - Drain Current (A)

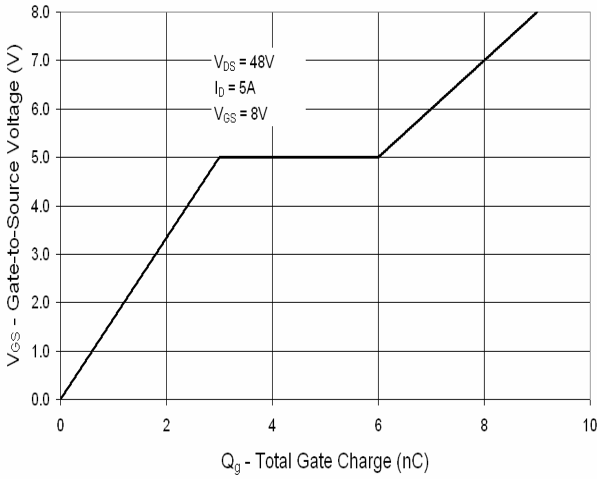

On State Resistance vs. Junction Temperature
VGS = 8V
ID = 5A
rDS(on) - On State Resistance (Normalized)
TJ - Junction Temperature (°C)

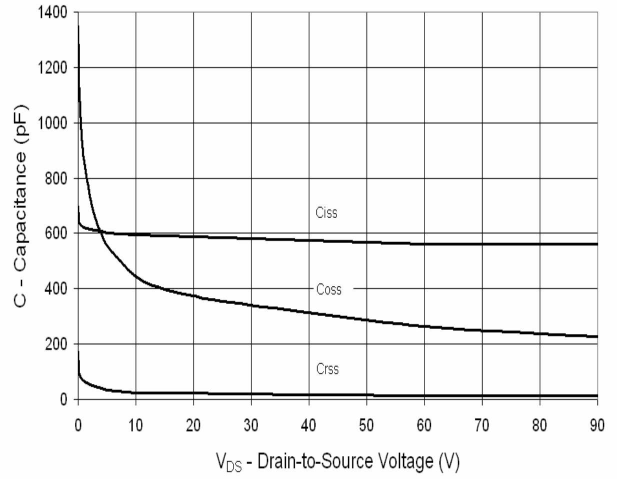

On-Resistance vs. Gate-to-Source Voltage
ID = 5A
RDS(on) - On State Resistance (Ω)
VGS - Gate-to-Source Voltage (V)

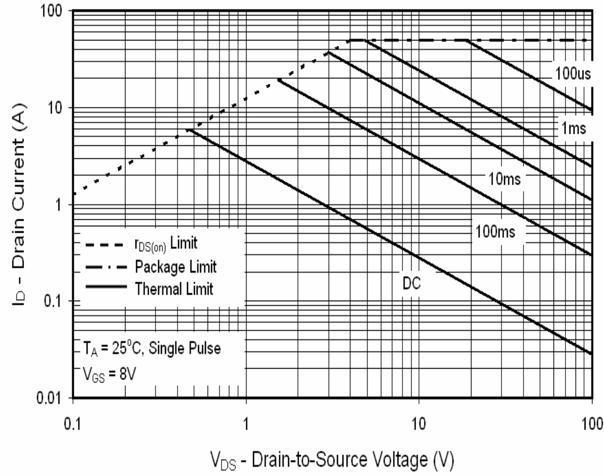

Gate Threshold Voltage vs. Junction Temperature
ID = 250uA
VGS(th) - Gate Threshold Voltage (Normalized)
TJ - Junction Temperature (°C)

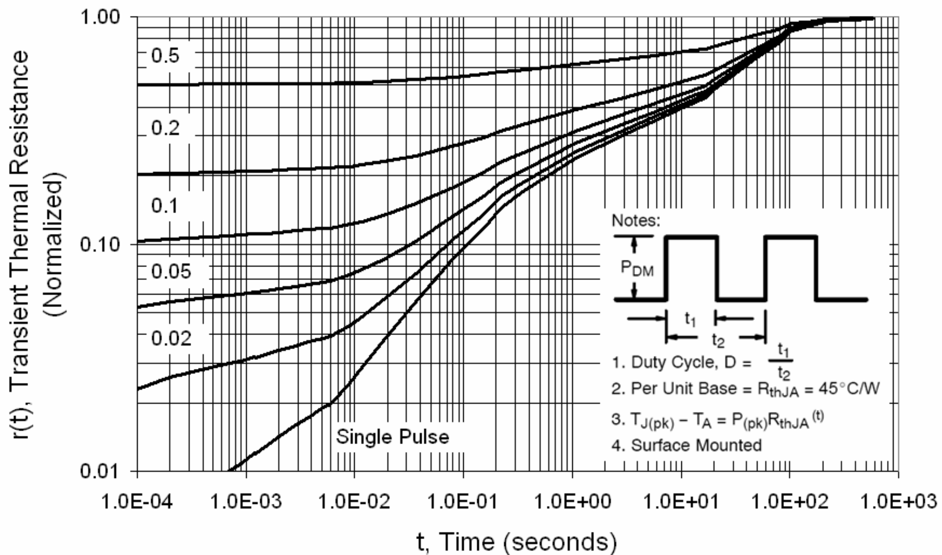

Source-Drain Diode Forward Voltage
TJ = 150°C
TJ = 25
IS - Source Current (A)
VSD - Diode Forward Voltage (V)

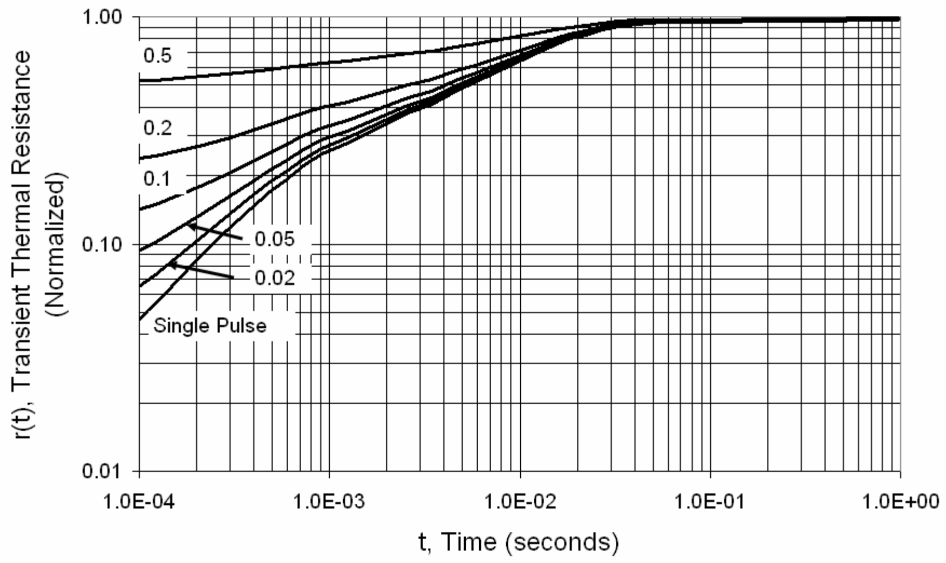

Drain-to-Source Breakdown Voltage vs. TJ
ID = 1mA
V(BR)DSS - Drain-to-Source Breakdown Voltage (Normalized)
TJ - Junction Temperature


Gate Charge
V_{DS} = 48V
I_D = 5A
V_{GS} = 8V
V_{GS} - Gate-to-Source Voltage (V)
Q_g - Total Gate Charge (nC)

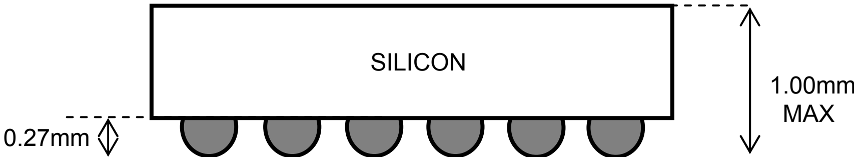

Capacitance
Ciss
Coss
Crss
C - Capacitance (pF)
V_{DS} - Drain-to-Source Voltage (V)

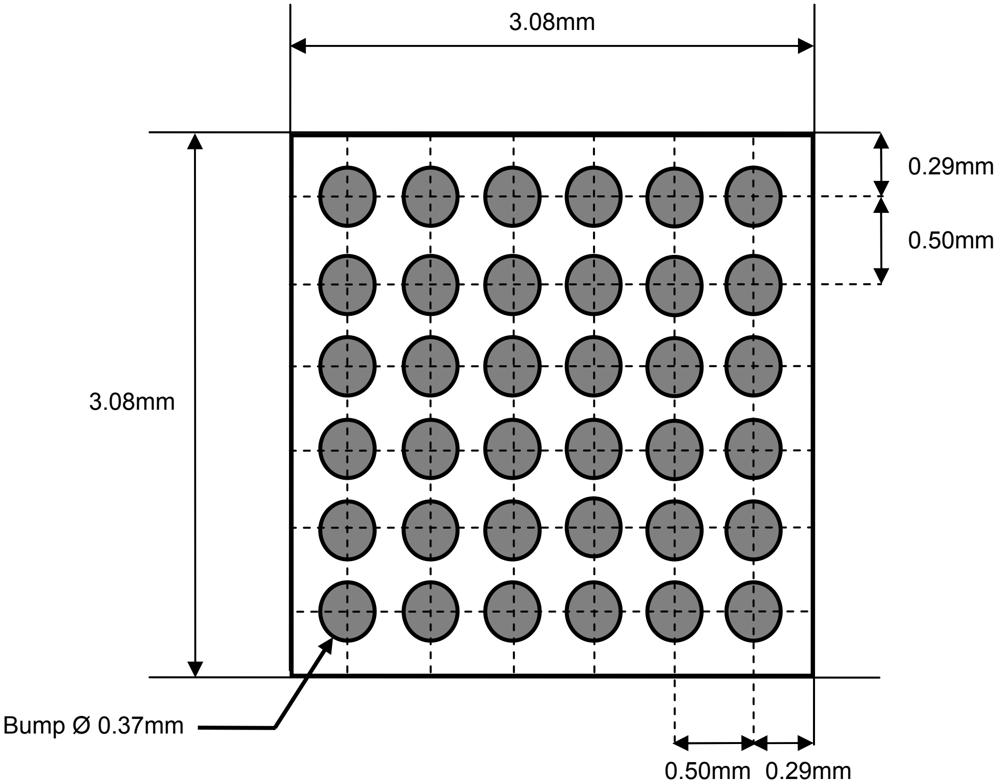

Maximum Rated Forward Biased Safe Operating Area
100us
1ms
10ms
100ms
DC
$r_{DS(on)}$ Limit
Package Limit
Thermal Limit
T_A = 25°C, Single Pulse
V_{GS} = 8V
I_D - Drain Current (A)
V_{DS} - Drain-to-Source Voltage (V)


Transient Thermal Response, Junction-to-Ambient
0.5
0.2
0.1
0.05
0.02
Single Pulse
Notes:
P_{DM}
t_1
t_2
1. Duty Cycle, D = $\frac{t_1}{t_2}$
2. Per Unit Base = R_{thJA} = 45°C/W
3. $T_{J(pk)} - T_A = P_{(pk)} R_{thJA}{}^{(t)}$
4. Surface Mounted
r(t), Transient Thermal Resistance (Normalized)
t, Time (seconds)


Transient Thermal Response, Junction-to-Ball
1.00
0.10
0.01
0.5
0.2
0.1
0.05
0.02
Single Pulse
r(t), Transient Thermal Resistance
(Normalized)
1.0E-04
1.0E-03
1.0E-02
1.0E-01
1.0E+00
t, Time (seconds)

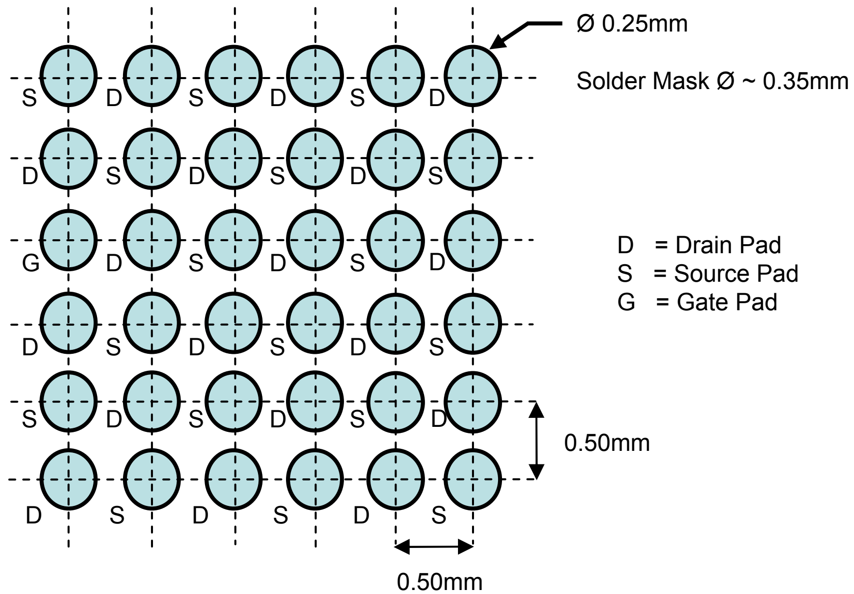
Dimensional Outline and Pad Layout



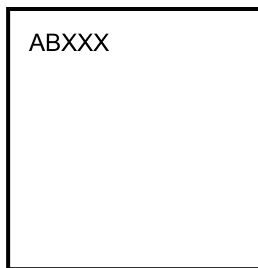


Bumps are Lead Free solder 96.8 Sn / 2.6 Ag / 0.6 Cu

Dimensional Outline and Pad Layout



LAND PATTERN
RECOMMENDATION



MARK ON BACKSIDE OF DIE

AB = GWS5N10 Product Code

XXXX = Date/Lot Traceability Code