



# GWS24N07 for Soft Switching

## Features

- Low RDS (on)
- Ultra low gate charge and figure of merit
- Patent Pending Lateral Power™ technology for High Frequency Switching
- Low Thermal Resistance Chip-Scale package  
Occupies 1/3rd the area of S08

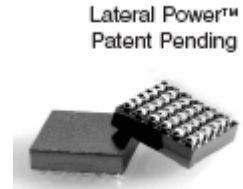
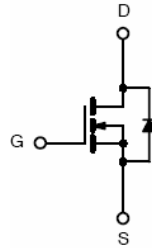
## Applications

- DC/DC Converters
- Portable Equipment
- OR'ing Diodes

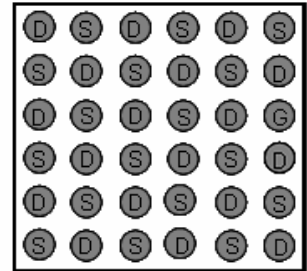
## Description

The GWS24N07 is an 8V, 1.25mΩ, chip-scale, N-Channel lateral MOSFET. The device uses Great Wall Semiconductor's patented Lateral Power™ technology that uniquely integrates low cost CMOS and wafer bumping fabrication processes. The MicroSurf™ chipscale package offers small size, low profile, and is fully compatible with standard SMT assembly processes. The GWS24N07 device offers unprecedented low on resistance and total gate charge, outperforming conventional trench MOSFETs and enabling high frequency, high efficiency synchronous rectification or low voltage switching. The device offers extremely high power density, reducing the board size of DC-DC converters and other power management systems.

Product Summary			
$I_D$	$T_A=25^\circ\text{C}$	24A	Max
$V_{(BR)DSS}$	$I_D=10\text{mA}$	8V	Max
$r_{DS(on)}$	$V_{GS}=4.5\text{V}$	1.25mΩ	Typ
$Q_g$	$V_{GS}=4.5\text{V}$	21nC	Typ



**Patent Pending**



**Bottom: Bump Side**

## Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	8	V	
Gate-Source Voltage	$V_{GS}$	+/- 8		
Drain Current	- Continuous	$I_D$	A	
	- Pulsed	$I_{DM}$		100
Single Pulse Avalanche Current	$T_{av} < 100\mu\text{S}$	$I_{AS}$	A	
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	$P_D$	2.8	W
	$T_A=70^\circ\text{C}$		1.8	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$	
Thermal Resistance <sup>a</sup>	- Junction-to-Ambient	$R_{thJA}$	45.0	$^\circ\text{C/W}$
	- Junction-to-Ball	$R_{thJB}$	2.0	

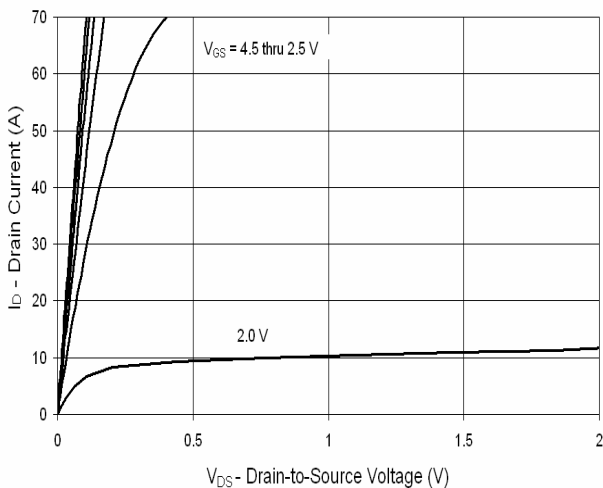
<sup>a</sup> When mounted on 1 inch square 2oz copper clad FR-4

# Electrical Characteristics

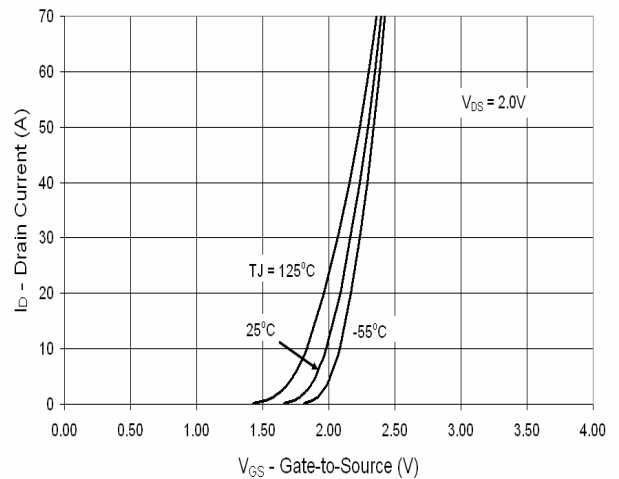
T<sub>J</sub>=25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =10mA	8			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =8V, V <sub>GS</sub> =0V			10	μA
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>GS</sub> =8V, V <sub>DS</sub> =0V			150	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.9		1.2	V
r <sub>DS(on)</sub>	Drain-to-Source On-State Resistance	V <sub>GS</sub> =4.5V, I <sub>D</sub> =24A		1.25	1.45	mΩ
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =8V, V <sub>GS</sub> =0V, f=1MHz		3000		pF
C <sub>oss</sub>	Output Capacitance			2500		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			500		pF
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =4.5V, I <sub>D</sub> =24A, V <sub>DS</sub> =6.4V		21	30	nC
Q <sub>gs</sub>	Gate-to-Source Charge			8		nC
Q <sub>gd</sub>	Gate-to-Drain Charge			2		nC
t <sub>rr</sub>	Source-to-Drain Reverse Recovery Time	I <sub>S</sub> =4A, di/dt=33A/μS		300		nS
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =4A, V <sub>GS</sub> =0V		0.75	1.0	V

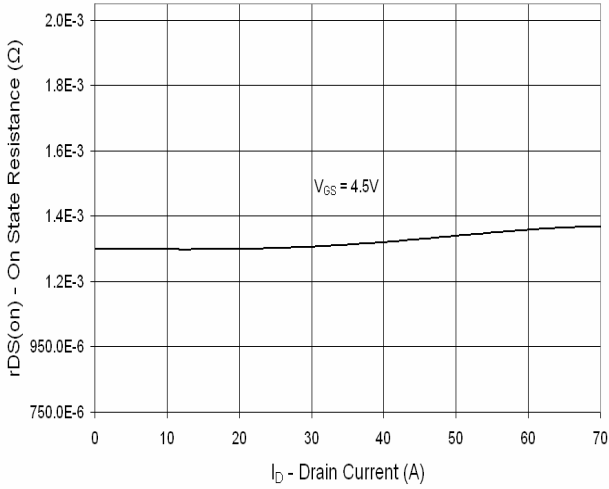
Output Characteristics



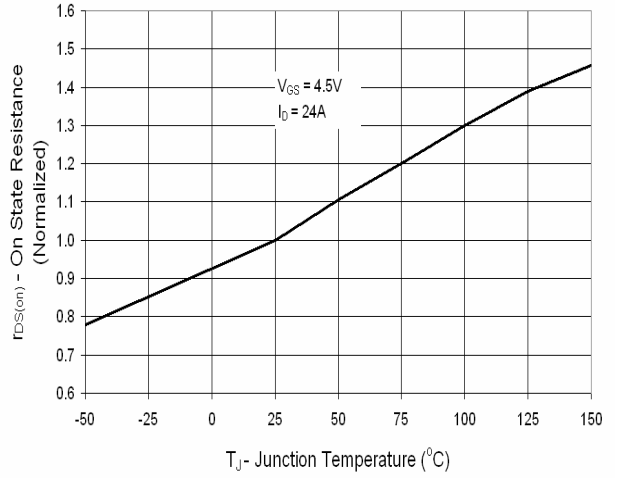
Transfer Characteristics



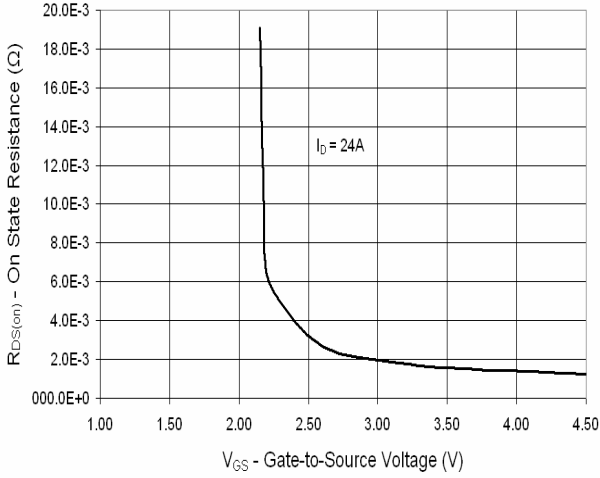
On State Resistance vs. Drain Current



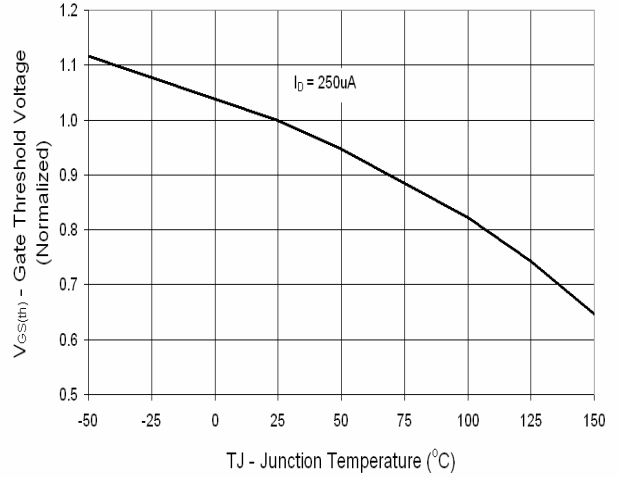
On State Resistance vs. Junction Temperature



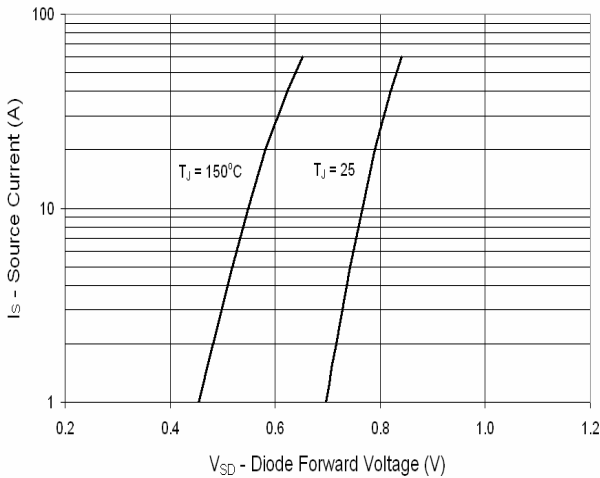
On-Resistance vs. Gate-to-Source Voltage



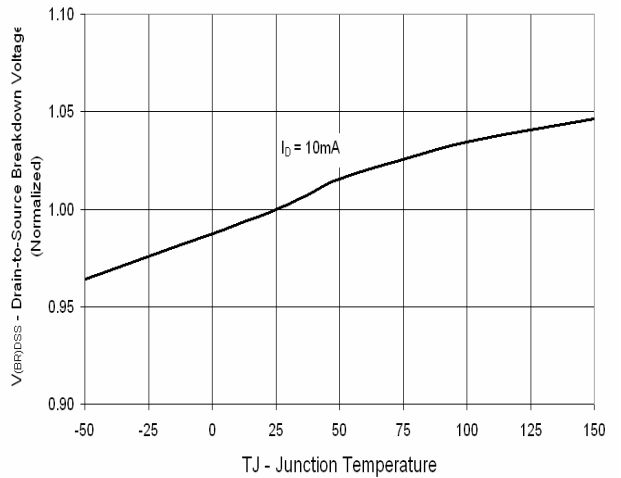
Gate Threshold Voltage vs. Junction Temperature



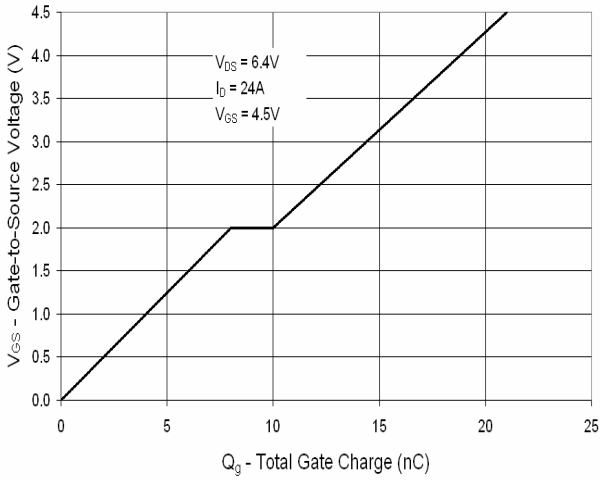
Source-Drain Diode Forward Voltage



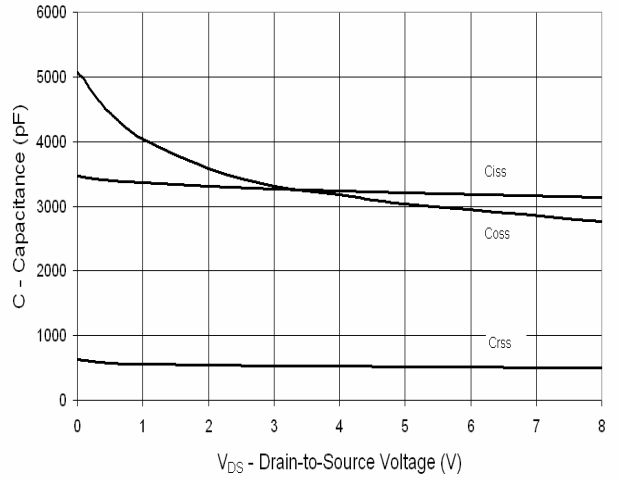
Drain-to-Source Breakdown Voltage vs. TJ



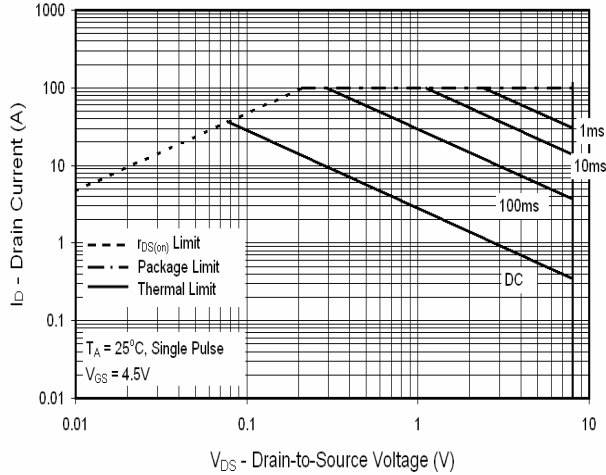
Gate Charge



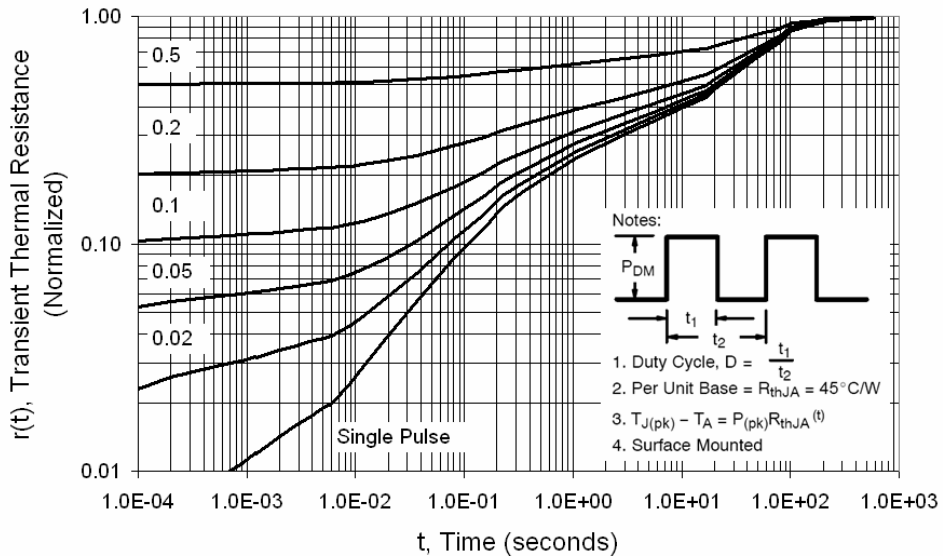
Capacitance



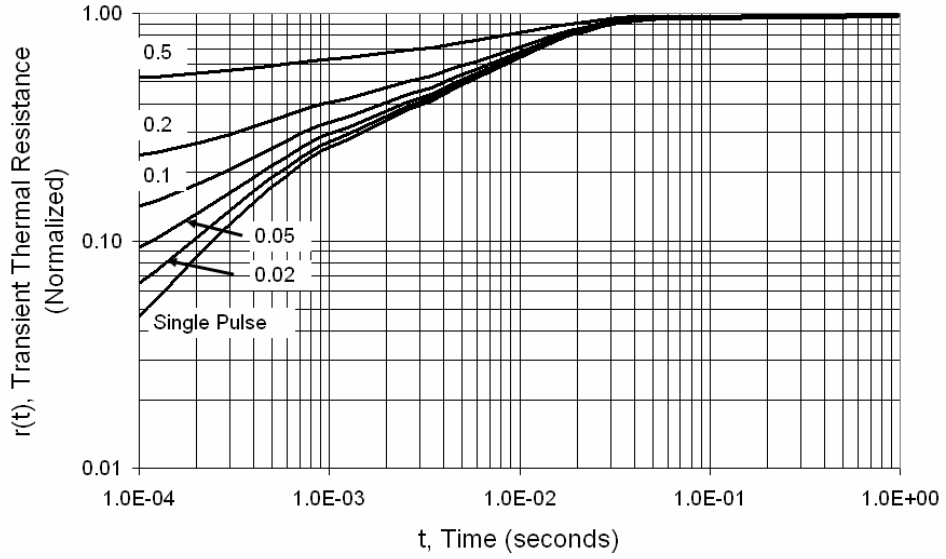
Maximum Rated Forward Biased Safe Operating Area



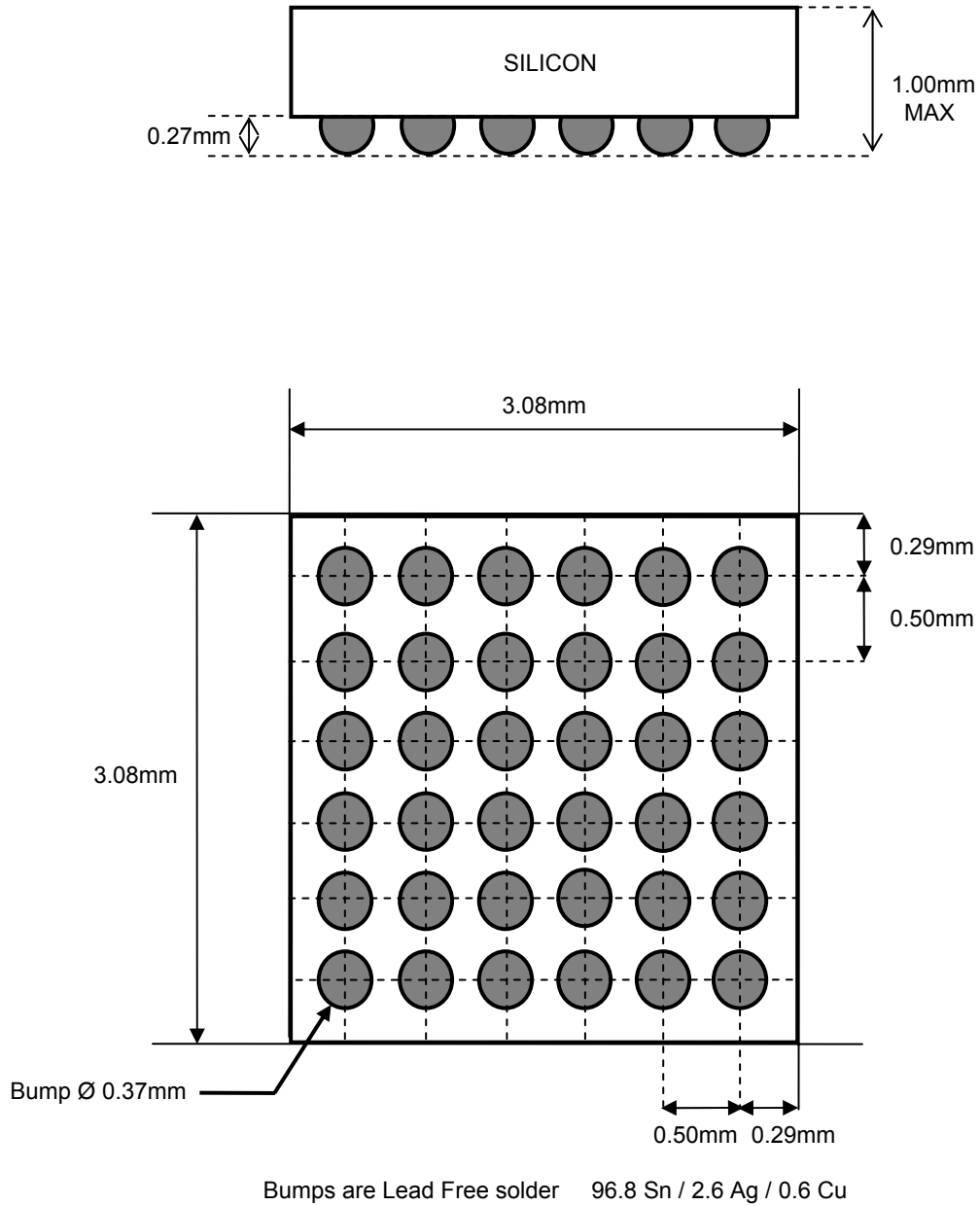
Transient Thermal Response, Junction-to-Ambient



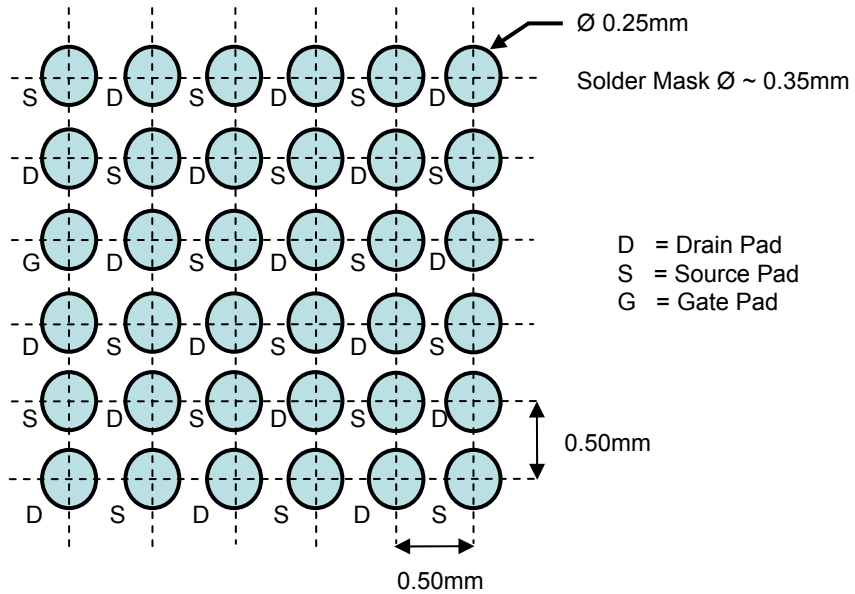
### Transient Thermal Response, Junction-to-Ball



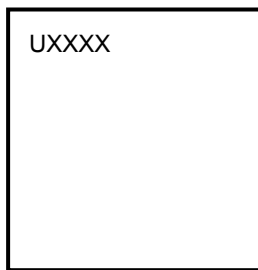
## Dimensional Outline and Pad Layout



## Dimensional Outline and Pad Layout



### LAND PATTERN RECOMMENDATION



MARK ON BACKSIDE OF DIE

U = GWS24N07 Product Code

XXXX = Date/Lot Traceability Code