



GWS12N07D for Soft Switching

Product Summary			
I_D	$T_A=25^\circ\text{C}$	12A	Max
$V_{(BR)DSS}$	$I_D=5\text{mA}$	8V	Max
$r_{DS(on)}$	$V_{GS}=3.3\text{V}$	2.6m Ω	Typ
Q_g	$V_{GS}=3.3\text{V}$	13nC	Typ

Features

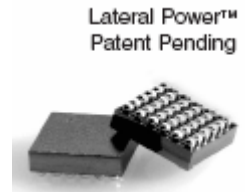
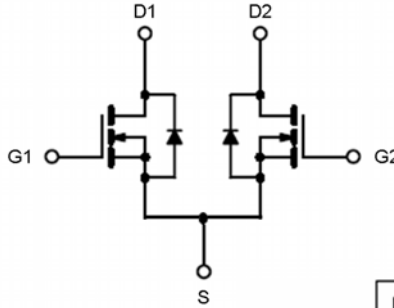
- Low RDS (on)
- Ultra low gate charge and figure of merit
- Patent Pending Lateral Power™ technology for High Frequency Switching
- Low Thermal Resistance Chip-Scale package Occupies 1/3rd the area of S08

Applications

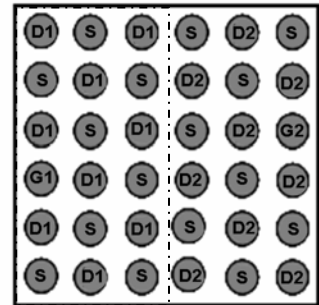
- DC/DC Converters
- Portable Equipment
- OR'ing Diodes

Description

The GWS12N07D is a Dual 8V, 2.6m Ω , chip-scale, N-Channel lateral MOSFET. The device uses Great Wall Semiconductor's patented Lateral Power™ technology that uniquely integrates low cost CMOS and wafer bumping fabrication processes. The MicroSurf™ chipscale package offers small size, low profile, and is fully compatible with standard SMT assembly processes. The GWS12N07D device offers unprecedented low on resistance and total gate charge, outperforming conventional trench MOSFETs and enabling high frequency, high efficiency synchronous rectification or low voltage switching. The device offers extremely high power density, reducing the board size of DC-DC converters and other power management systems.



Patent Pending



Bottom: Bump Side

Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	8	V	
Gate-Source Voltage	V_{GS}	+/- 5		
Drain Current ($I_{D1} + I_{D2}$)	- Continuous	I_D	A	
	- Pulsed	I_{DM}		100
Single Pulse Avalanche Current ($I_{D1} + I_{D2}$)	$T_{av} < 100\mu\text{S}$	I_{AS}	A	
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.8	W
	$T_A=70^\circ\text{C}$		1.8	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$	
Thermal Resistance ^a	- Junction-to-Ambient	R_{thJA}	45.0	$^\circ\text{C/W}$
	- Junction-to-Ball	R_{thJB}	2.0	

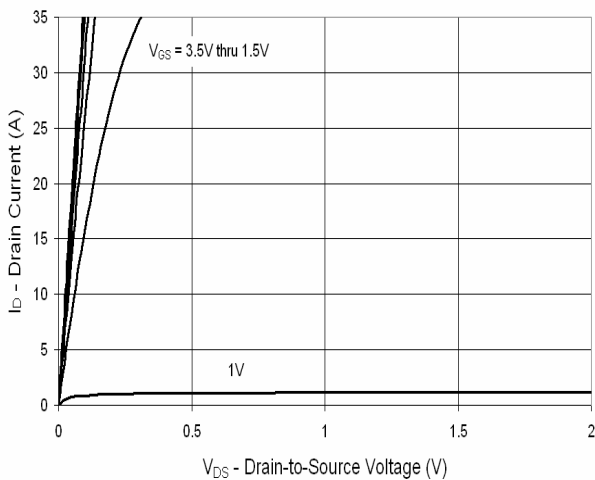
^a When mounted on 1 inch square 2oz copper clad FR-4

Electrical Characteristics (Single MOSFET)

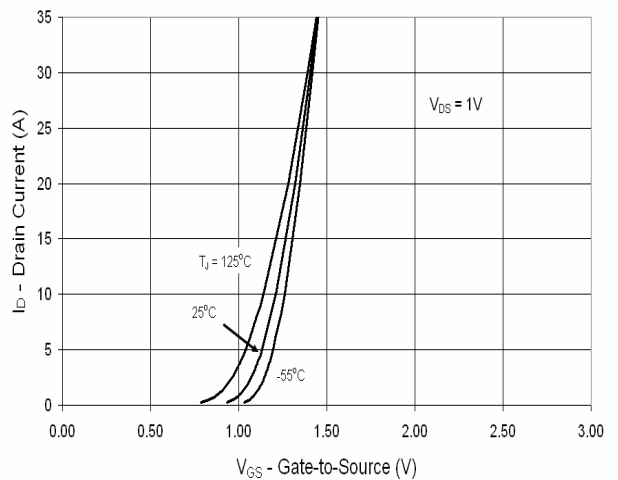
$T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS}=0V, I_D=5mA$	8			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=7V, V_{GS}=0V$			10	μA
I_{GSS}	Gate-Body Leakage	$V_{GS}=5V, V_{DS}=0V$			150	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.4		0.8	V
$r_{DS(on)}$	Drain-to-Source On-State Resistance	$V_{GS}=3.3V, I_D=12A$		2.6	2.8	$\text{m}\Omega$
C_{iss}	Input Capacitance	$V_{DS}=8V, V_{GS}=0V, f=1\text{MHz}$		1900		pF
C_{oss}	Output Capacitance			1300		pF
C_{rss}	Reverse Transfer Capacitance			275		pF
Q_g	Total Gate Charge	$V_{GS}=3.3V, I_D=12A, V_{DS}=6.4V$		13	20	nC
Q_{gs}	Gate-to-Source Charge			3		nC
Q_{gd}	Gate-to-Drain Charge			1.5		nC
t_{rr}	Source-to-Drain Reverse Recovery Time	$I_S=4A, di/dt=33A/\mu\text{S}$		300		nS
V_{SD}	Diode Forward Voltage	$I_S=4A, V_{GS}=0V$		0.75	1.0	V

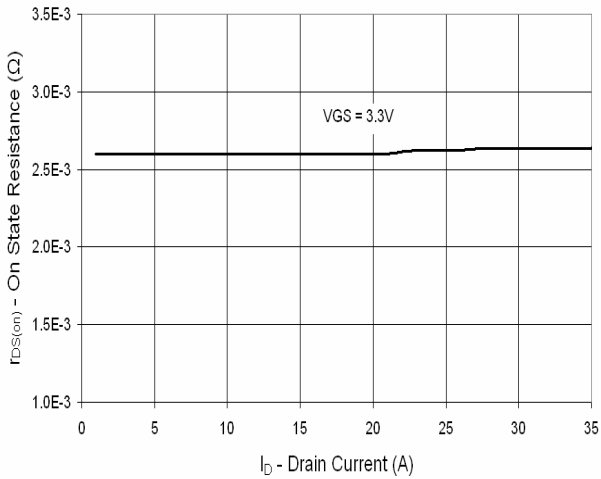
Output Characteristics



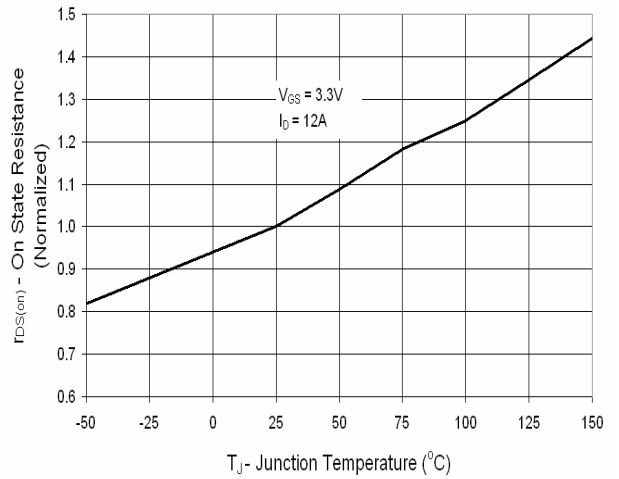
Transfer Characteristics



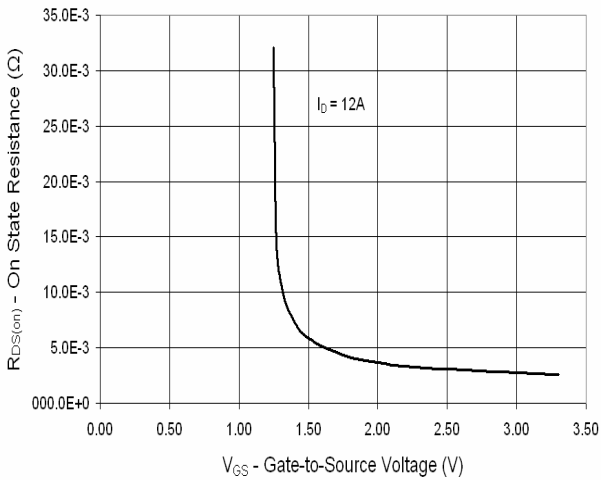
On Resistance vs. Drain Current



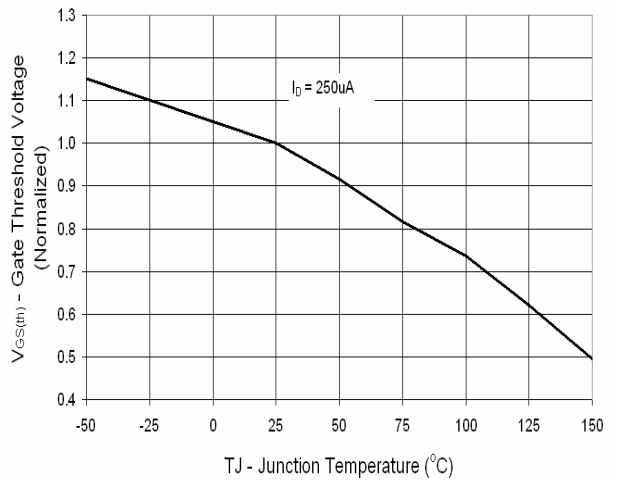
On State Resistance vs. Junction Temperature



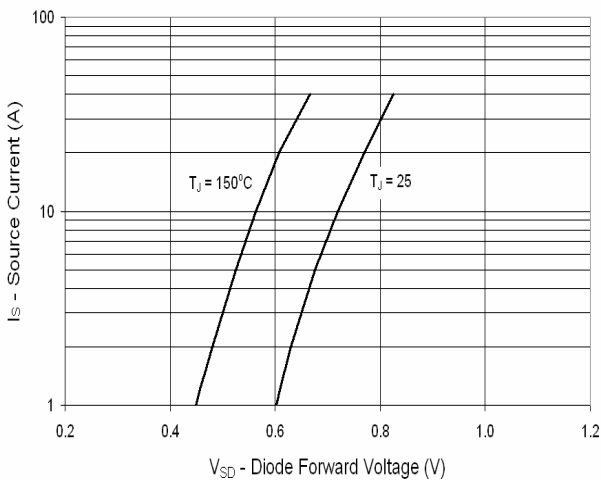
On-Resistance vs. Gate-to-Source Voltage



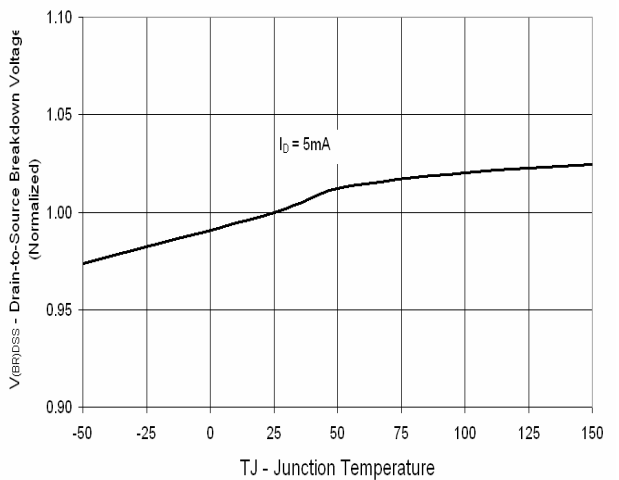
Gate Threshold Voltage vs. Junction Temperature



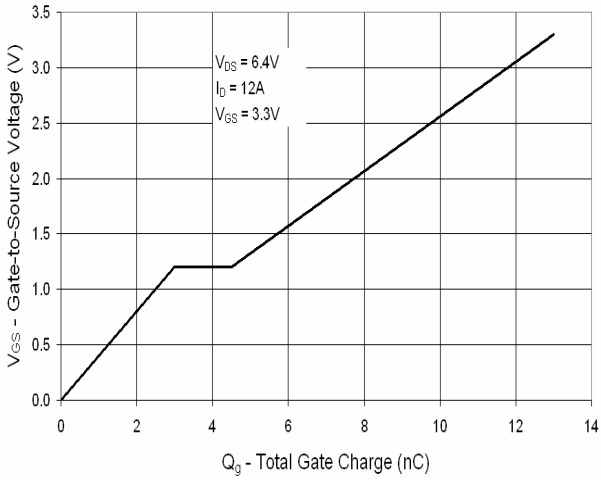
Source-Drain Diode Forward Voltage



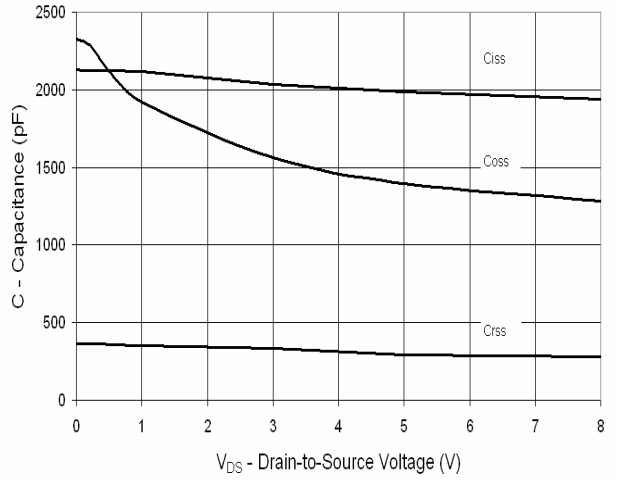
Drain-to-Source Breakdown Voltage vs. T_J



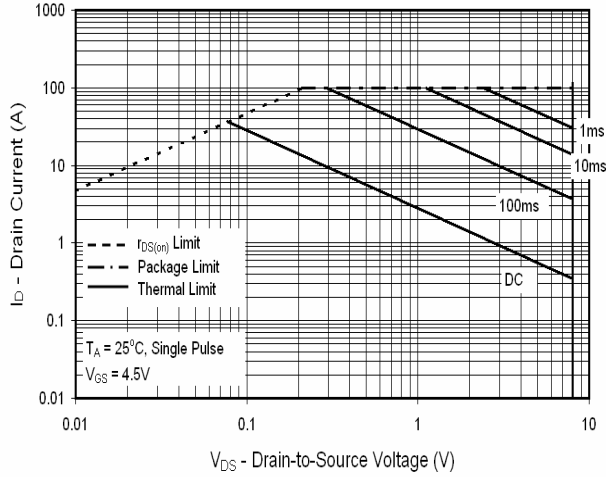
Gate Charge



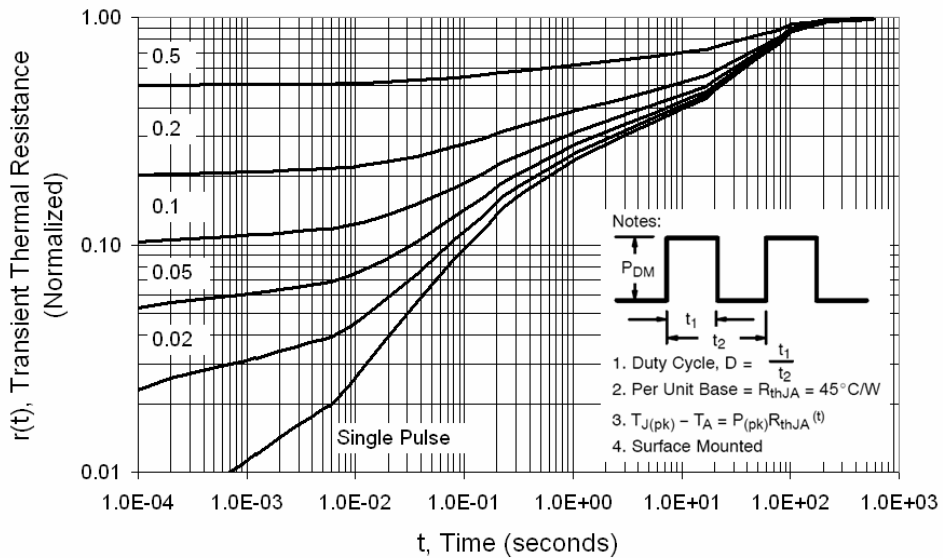
Capacitance



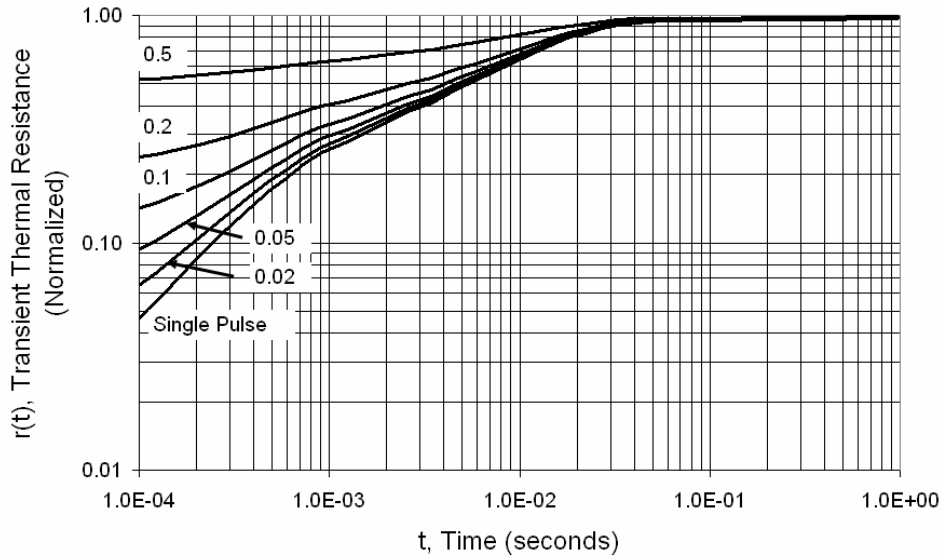
Maximum Rated Forward Biased Safe Operating Area



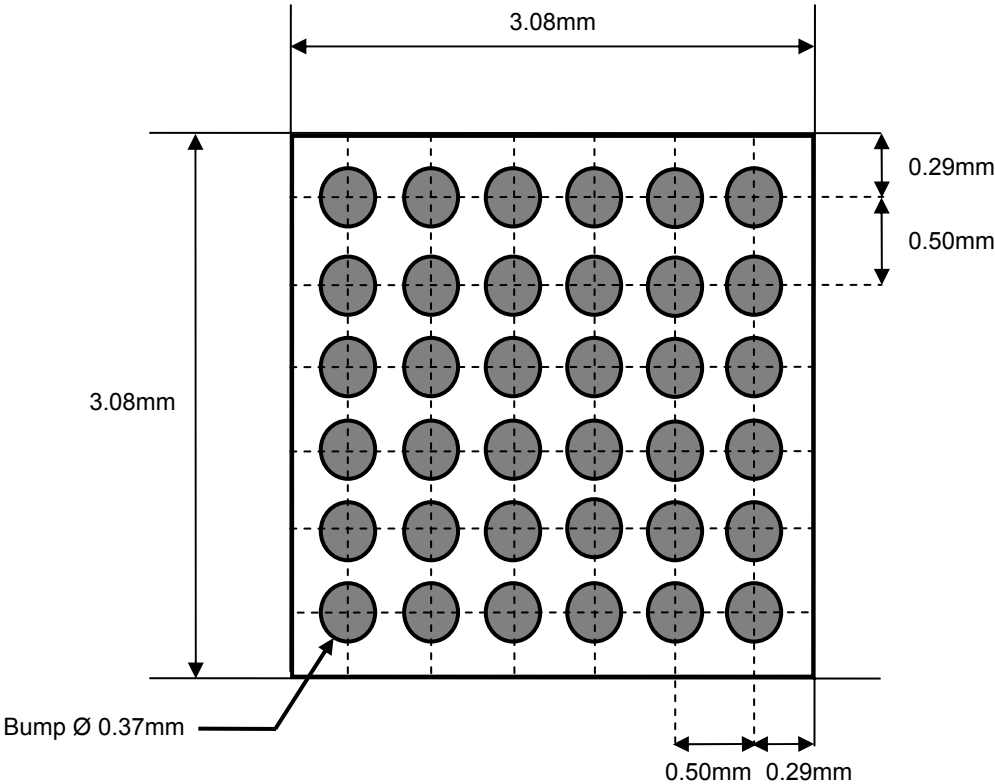
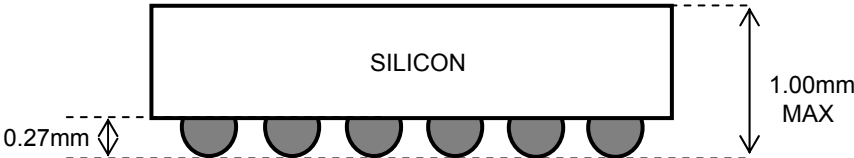
Transient Thermal Response, Junction-to-Ambient



Transient Thermal Response, Junction-to-Ball

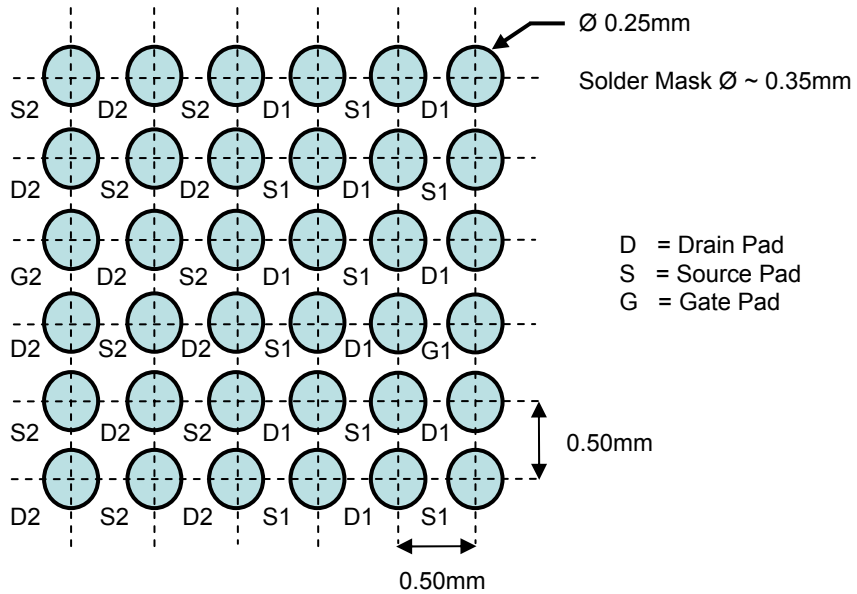


Dimensional Outline and Pad Layout



Bumps are Lead Free solder 96.8 Sn / 2.6 Ag / 0.6 Cu

Dimensional Outline and Pad Layout



LAND PATTERN
RECOMMENDATION



MARK ON BACKSIDE OF DIE

V = GWS12N07D Product Code

XXXX = Date/Lot Traceability Code