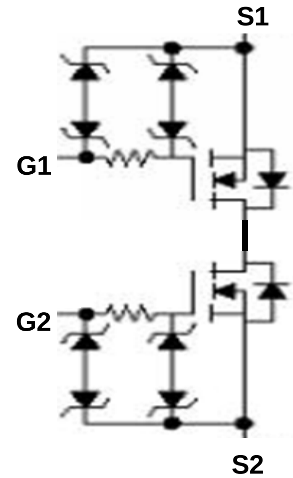
GWS7302E Dual N-Channel MOSFET



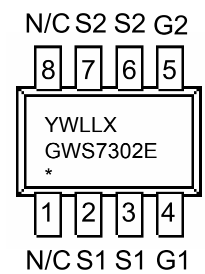
General Description

The GWS7302E is a dual low threshold gate protected MOSFET designed for the small battery, cell phone, and PDA markets. Using ultra high density MOSFET process and space saving small outline J-lead package, performance normally found in a TSSOP8 footprint has been squeezed into the footprint of a TSOP6 package.

Features

- 4.5A, 20V $r_{DS(ON)}$ = 24mΩ typ. at 4.5 Volts
- 3.8A, 20V $r_{DS(ON)}$ = 34mΩ typ. at 2.5 Volts
- Excellent thermal characteristics.
- Rated for High Electrical Overstress Performance of 15A short circuit and over current.
- Integrated gate diodes provide Electro-Static Discharge (ESD) protection of 2500V HBM.

TSOPJW-8 Package



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current[1]		I_D	4.5	A
Pulsed Drain Current[2]		I_{DM}	30	
Maximum Power Dissipation[1]	T_A=25°C	P_D	1	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance[3]	t < 10 sec	R_{thJA}	83	°C/W
	Steady-State	R_{thJA}	120	
Junction-to-Foot (Drain) Thermal Resistance[3]		R_{thJF}	70	

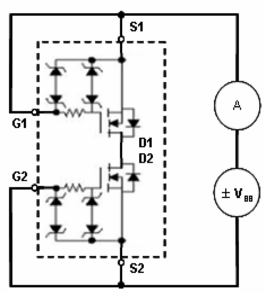
Notes: 1. Surface mounted on FR4 board. t < 10 s.
2. Pulse test; pulse width < 300 us, duty cycle <2%.
3. Surface mounted on FR4 board.

Electrical Characteristics (T_J = 25 °C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static[1]						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	20	-	-	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 4.5A	-	24	32	mΩ
		V_{GS} = 2.7V, I_D = 3.8A	-	34	45	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.6	1.0	1.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V, V_{DS} = 16V	-	-	1	uA
Gate Body Leakage	I_{GSS}	V_{DS} = 0V V_{GS} = ±8V	-	-	100	nA
Forward Transconductance	gfs	V_{DS} = 10V, I_D = 2.5A	-	19	-	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 4.5A, V_{GS} = 4.5V	-	7		nC
Gate-Source Charge	Q_{gs}		-	1.5	-	
Gate-Drain Charge	Q_{gd}		-	2.3	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, I_D = 1A, V_{GEN} = 4.5V, R_G = 4.7 ohms	-	7		nS
TurnOn Rise Time	t_r		-	33		
Turn-Off Delay Time	$t_{d(off)}$		-	27		
Turn-Off Fall Time	t_f		-	10		
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V, f = 1 MH_Z	-	650	-	
Output Capacitance	C_{oss}		-	150	-	
Reverse Transfer Capacitance	C_{rss}		-	90	-	
Source Drain Diode[1]						
Diode Forward Voltage	V_{SD}	I_S = 1.5A, V_{GS} = 0V	-	0.71	1.2	V

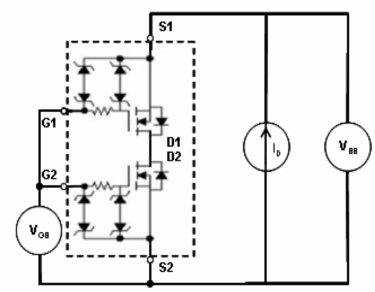
Note: 1. Pulse test; pulse width < 300 us, duty cycle <2%.

Test Circuit 1: I_{DSS}, Zero Gate Voltage Drain Current



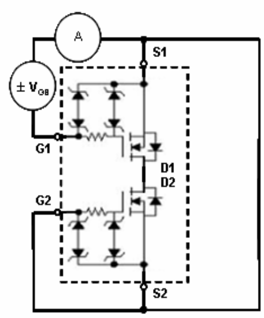
FET (1) I_{DSS}: VS2=VG2=20V, VS1=VG1=0V
FET (2) I_{DSS}: VS1=VG1=20V, VS2=VG2=0V

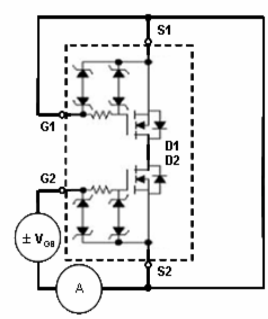
Test Circuit 2: $R_{DS(ON)}$, Drain-to-Source ON State Resistance



FET (1 or 2) $R_{DS(ON)} = (V_{SS} / I_D) / 2$

Test Circuit 3: I_{GSS}, Gate Body Leakage

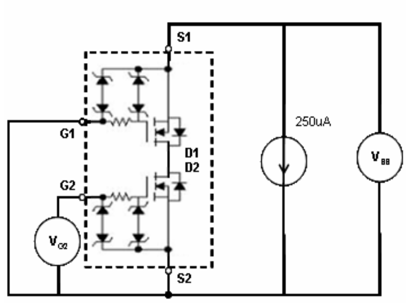


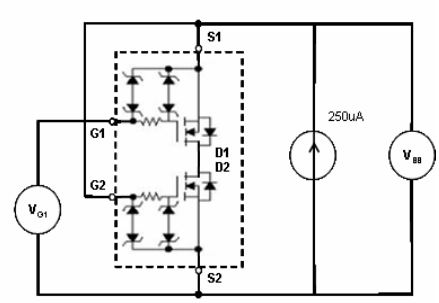


FET (1) I_{GSS}: $V_{GS1} = \pm 12V$, $V_{S1} = V_{S2} = V_{G2} = 0V$

FET (2) I_{GSS}: $V_{GS2} = \pm 12V$, $V_{S1} = V_{S2} = V_{G1} = 0V$

Test Circuit 4: $V_{GS(th)}$, Gate Body Leakage

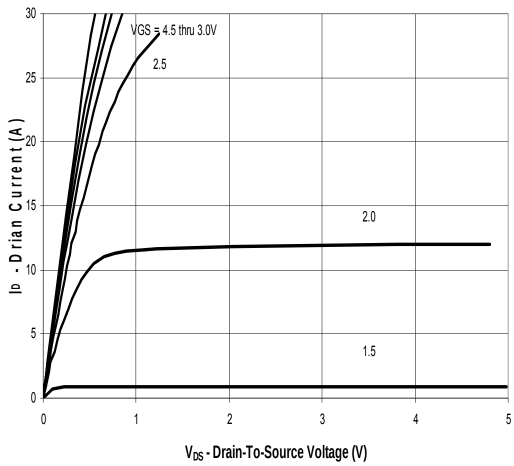




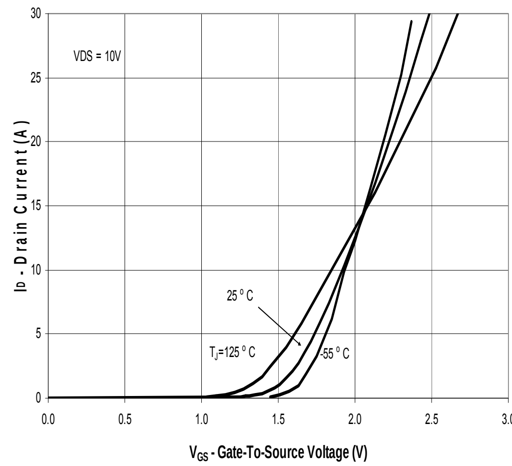
FET (1) $V_{GS(th)1}$ **= Vss**
Where: $V_{G1} = V_{S2}$, $V_{S1} = 0V$, $V_{G2} = 4.5V$, $I_{SS} = 250uA$

FET (2) $V_{GS(th)2} = V_{SS}$
Where: $V_{G2} = V_{S2}$, $V_{S2} = 0V$, $V_{G1} = 4.5V$, $I_{SS} = 250uA$

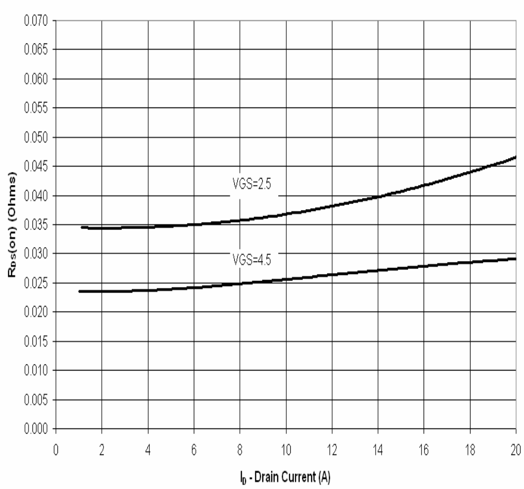
Output Characteristics



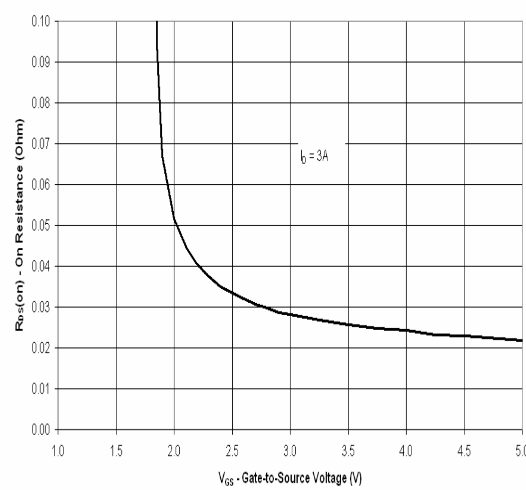
Transfer Characteristics



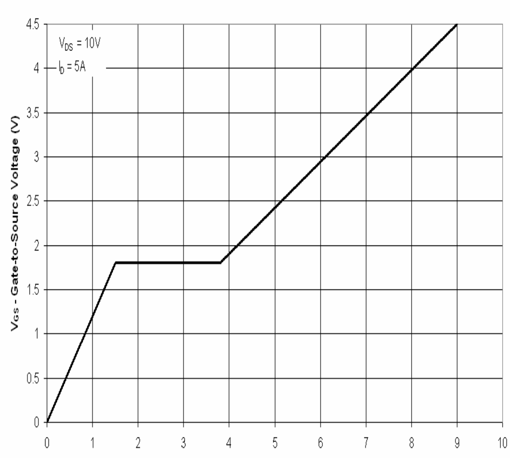
On Resistance Vs. Drain Current



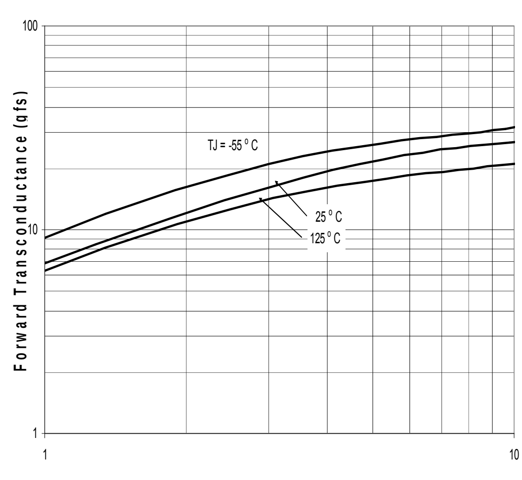
On Resistance Vs. Gate-to-Source Voltage



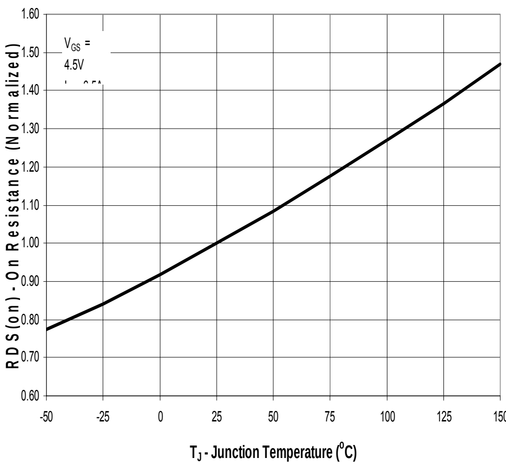
Gate Charge



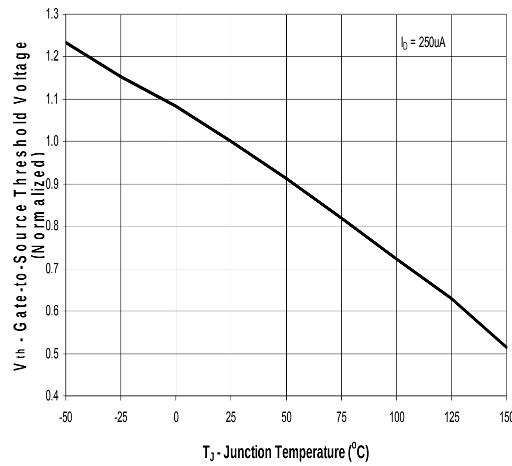
Forward Transconductance Vs. Drain Current



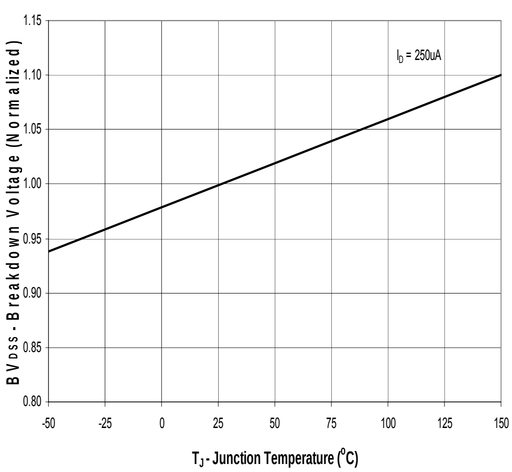
On Resistance Vs. Junction Temperature



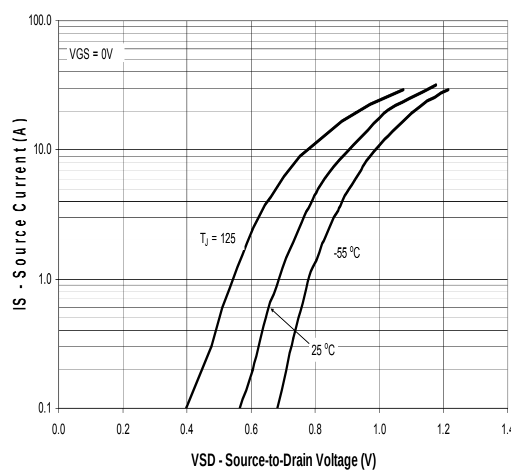
Threshold Voltage Vs. Temperature



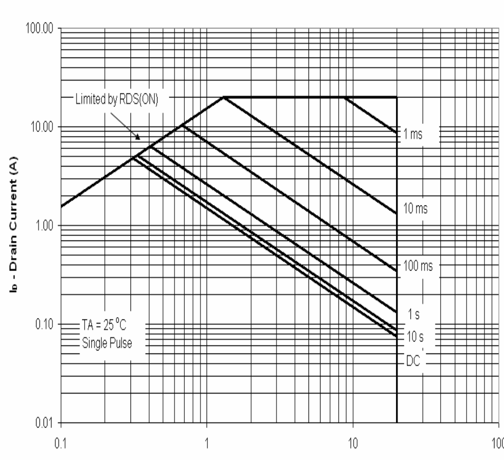
Breakdown Voltage Vs. Junction Temperature



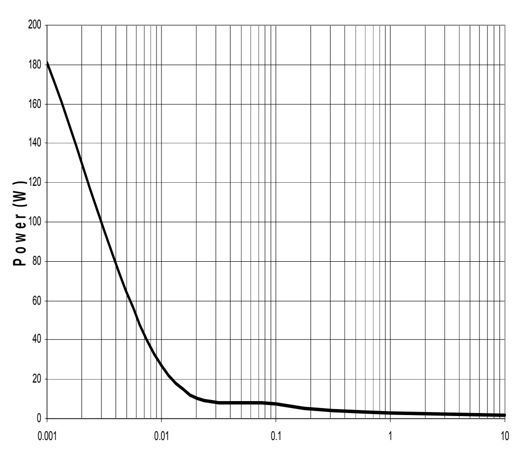
Source Drain Diode Forward Voltage



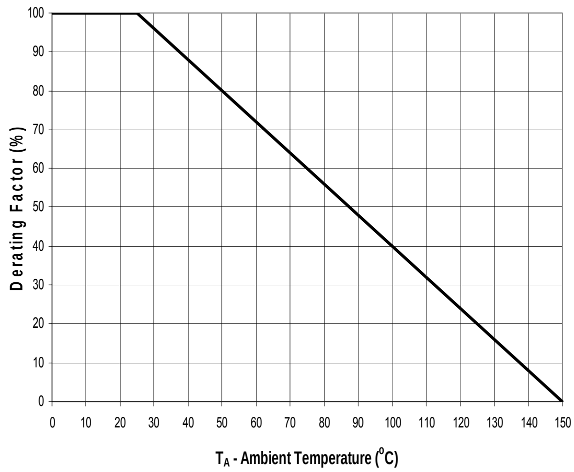
Safe Operating Area, Junction-to-Ambient



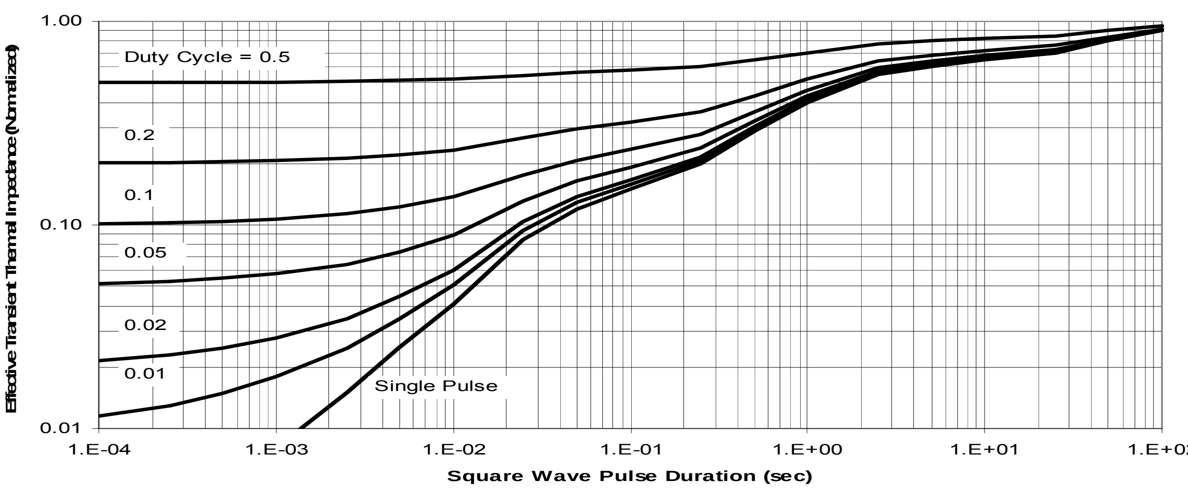
Single Pulse Power



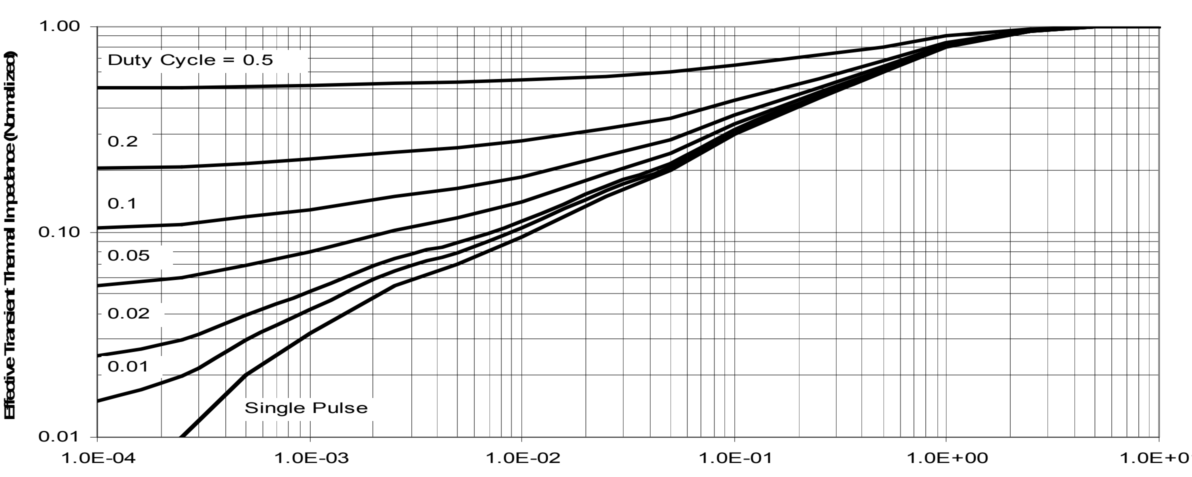
Derating Factor for Forward Bias Safe Operating Area



Normalized Transient Thermal Impedance, Junction-to-Ambient



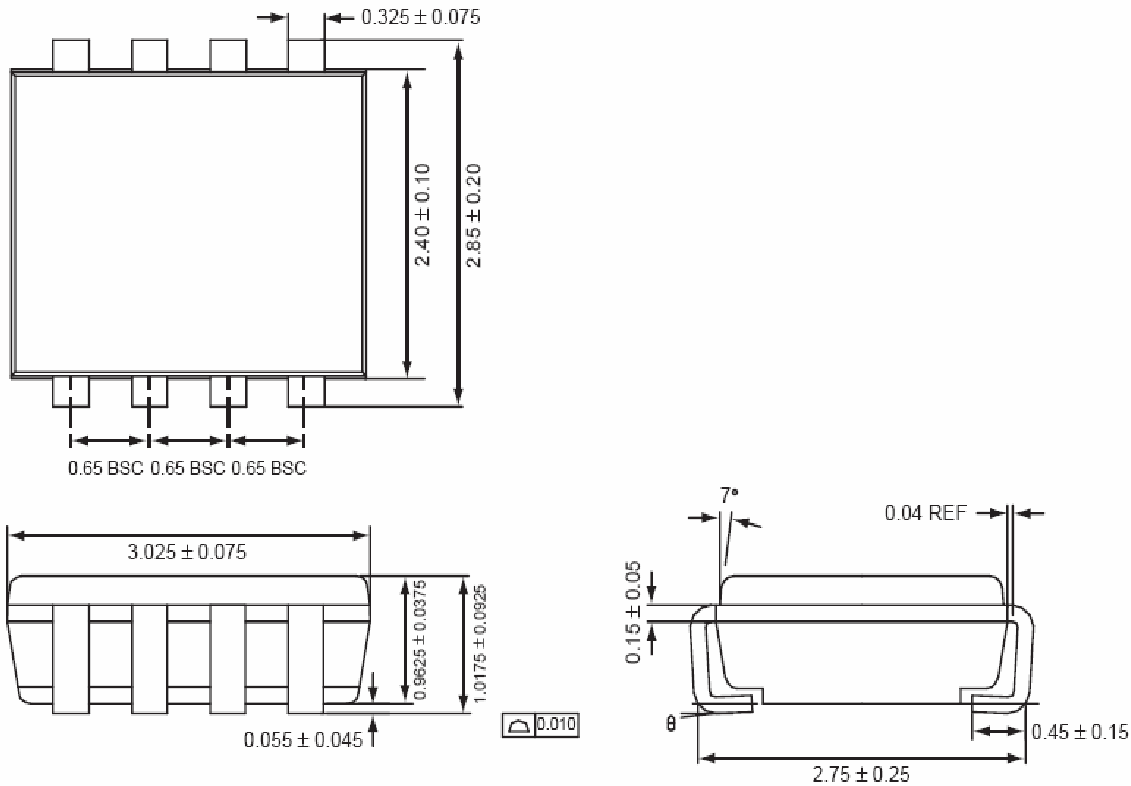
Normalized Transient Thermal Impedance, Junction-to-Foot



Ordering Information

Package = TSOPJW-8
Marking = as agreed.
Part Number = GWS7302EITS-T1 for Tape and Reel

Package Information



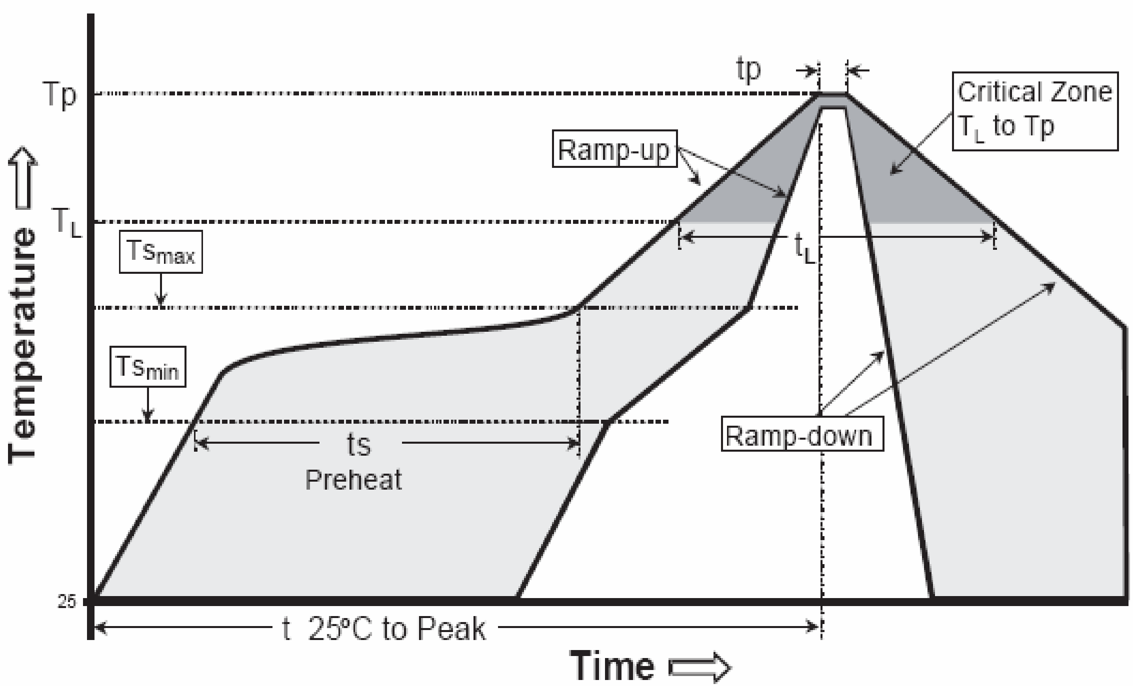
Reflow Profile Classification

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	240^{O}C	260^{O}C
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

2: GWS devices can be reflowed a max of 2 times when mounted using our recommended reflow conditions.

3: When repairing after solder reflow, complete with-in 10 seconds for iron temperatures of up to 260^{O}C.



General Precautions and Warnings

- The information in this document is subject to change without notice.
- Before using this document, confirm that this is the latest version.
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Great Wall Semiconductor.
- Great Wall Semiconductor assumes to responsibility for any errors that may appear in this document.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by Great Wall Semiconductor for any infringements of patents or other rights of the third parties which may result from its use.
- While Great Wall Semiconductor endeavors to enhance the quality, reliability and safety of it's products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely.
- To minimize the risks of damage to property or injury (including death) to persons arising from defects in Great Wall Semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire containment and anti-failure features.
- When the device listed in this document is intended for usage in Lithium Ion Battery charge and discharge control applications, special precautions must be employed by the customer to prevent device damage should a short circuit occur. For example, a PTC Thermistor can be used by the customer to shut off the power supply if a short-circuit occurs. If the power supply is not shut off during a short circuit, a large short circuit current will flow which may cause the device to catch fire or smoke.