APPLICATION NOTE: AN – 504
For information only

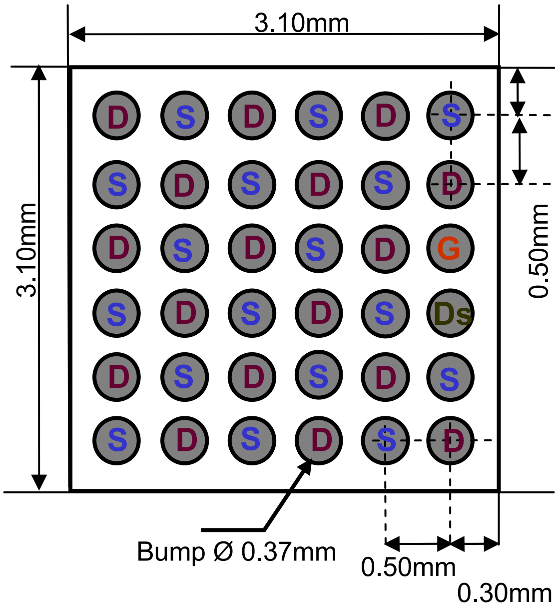
BGA Package Design and Printed Circuit Board Guidelines for Great Wall Semiconductor's GWS12N30 lateral MOSFET

General Description

This application note provides guidelines for integrating Great Wall Semiconductor's new low cost, state of the art MicroSurf™ MOSFETs (Figure 1) into standard PCB assemblies. A multilayer layer structure is described for paralleled devices, allowing for optimal thermal and electrical performance. All critical dimensions are specified and processing guidelines are given.

Printed Circuit Board Design

To achieve optimal performance, this device should be mounted on a FR-4 or Polyimide PCB compliant with IPC-A-610 standards. The drain and sense pad array is designed in an alternating fashion, as shown in Figure 2. Therefore, to minimize thermal resistances and voltage drops, the routing and via structure of the various layers need to take this into consideration.



Bumps are Lead Free solder
96.8 Sn / 2.6 Ag / 0.6 Cu

Figure 2. Die Dimensions: Bottom view , bump side

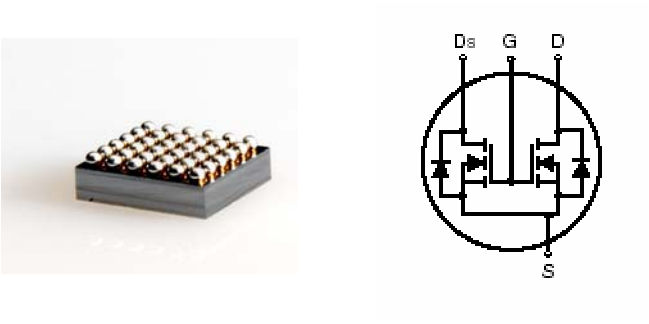


Figure 1. 30V Single N-channel 4.5V Specified Lateral Power™

Ball Grid Array Land Design

Two types of land design pads can be used, each having advantages and disadvantages. The first is a solder mask defined (SMD) land pad. This is characterized by having the solder mask opening that is slightly smaller than the copper pad underneath it. Thus it is the solder mask that defines precisely where the solder makes contact with the copper pad. In this approach, only the top side of the copper pad contacts the solder. Figure 3. depicts the SMD land pad.

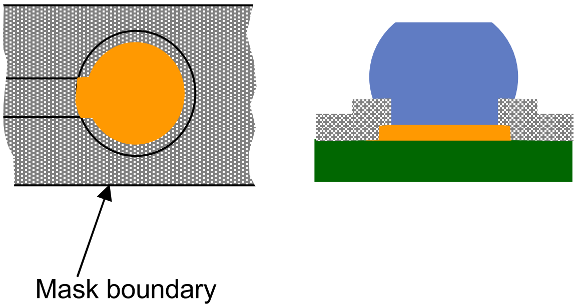


Figure 3. Top and cross sectional views of SMD land pad.

The second soldering approach is a non-solder mask defined (non-SMD) land pad. This method provides a mask opening that is larger than the copper pad. Thus the solder is free to flow beyond the boundary of the copper pad as it reflows. In this approach, both the top side of the copper pad contact as well as its sides can contact the solder. Figure 4. depicts the non-SMD land pad.

Generally, the SMD approach provides better adhesion of the copper to the pcb laminate surface. However, it has been shown that the fatigue life of the non-SMD approach is improved vs. the SMD method.

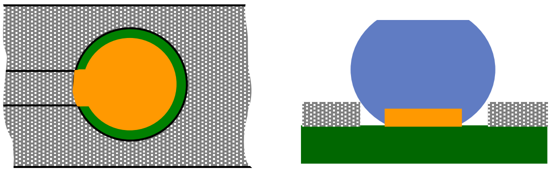
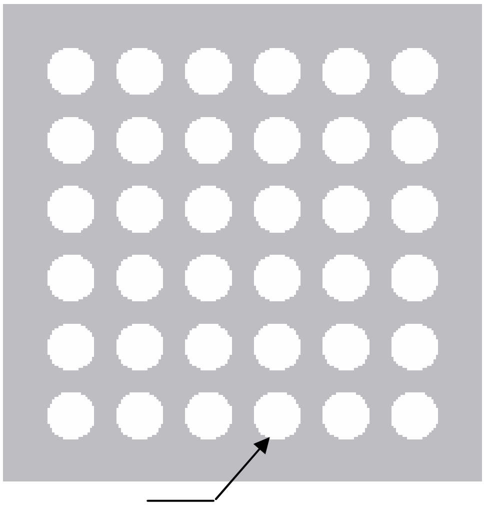


Figure 4. Top and cross sectional views of Non-SMD land pad.

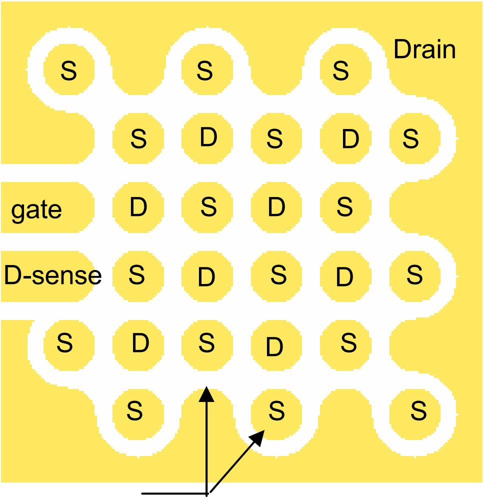
Pad Arrangement

To minimize parasitic losses, a multilayer pad arrangement is utilized to take advantage of the alternating Drain and Source pad placement. Vias are appropriately placed between the various layers. Figure 5 shows the solder mask and three metal layers along with via locations.



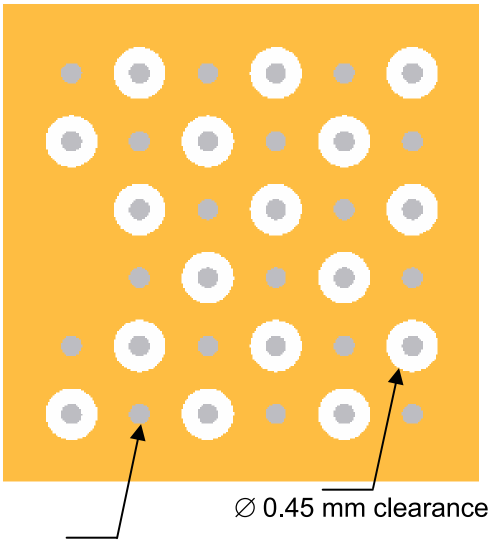
∅ 0.35mm for SMD
∅ 0.38mm for Non-SMD

Figure 5a. Solder Mask layer



∅ 0.38mm for SMD
∅ 0.30mm for Non-SMD

Figure 5b. Top Metal layer (Layer 1)



∅ 0.45 mm clearance

∅0.16mm Vias from between Layers 1 and 2

Figure 5c. Top Metal layer (Layer 2)

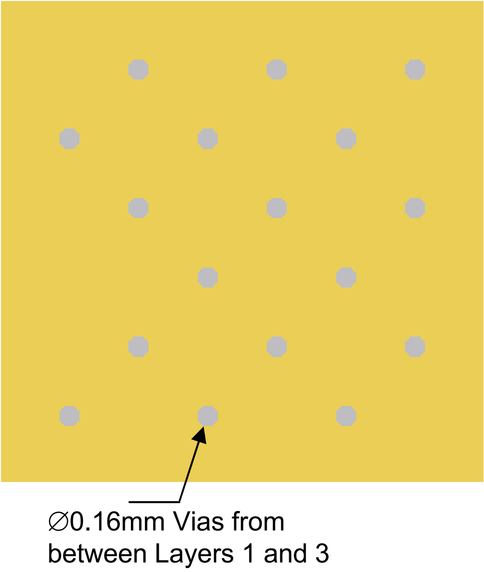


Figure 5d. Top Metal layer (Layer 3)

Via Design

Directly beneath the device, there are two sets of vias connecting layers 1-2 and 1-3. These have a nominal diameters of 0.16 mm, and can be plated shut. When integrating the device into a pcb design, there can be other vias located outside the boundaries of the die. These can have larger diameters and are used to reduce both electrical and thermal resistances.   Figure 6 depicts the cross section of the vias located within the boundaries of the MOSFET die.

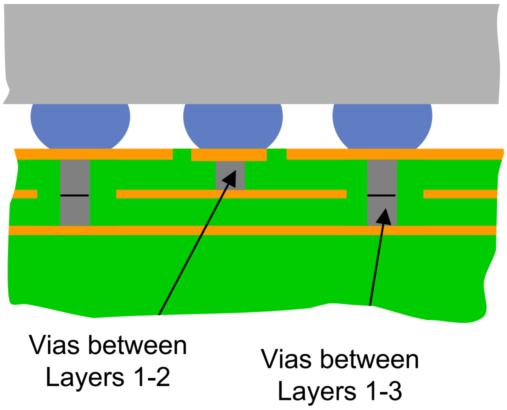


Figure 6. Via Structure

Soldering

There are various considerations with respect to processing and assembly.   Although the device can be soldered with the aid of only a flux material, it is also possible to use a solder paste. This can aid the assembly process by holding the BGA more securely in place and can compensate for any planarity variations in the solder balls.   A proper thermal profile should be used consistent with the selected solder. A Type 3 or finer (no clean) solder paste is recommended.

Stencil Fabrication

Solder paste deposition using a stencil printing process involves pressurized application of solder paste through predefined apertures. Three general methods exist for stencil fabrication: chemical etching, laser cutting, and nickel plate-up. While all three have advantages in stencil PCB component-attach manufacturing, not all are suitable for generating fine pitch (0.5mm) bump-attach stencils. Chemical etching cannot support the fine geometries and tolerances required for CSP stencils, and is not considered a viable process for producing them.

For laser-cut stencils, a thin stainless-steel foil is held flat while the apertures are cut with a high-powered laser. The observed tight tolerances on aperture dimensions, combined with smooth sidewalls, makes laser cutting stencils a desirable and popular process. However, the cost of laser-cut stencils increases with the number of apertures.

In the nickel plate-up process, the stencil is grown by plating nickel onto a mandrel through a patterned dry-film resist. This process also produces smooth sidewalls with tight shape and size tolerances. However, this process requires patterning and plating equipment that may increase the cost of stencil manufacturing.

The aperture design can be either square or round. In the case of square aperture openings, a size of 0.25mm x 0.25mm and 0.100mm depth may be used. Also, the corners must have at least a 50-micron radius. It is recommended to offset apertures from the copper pad to maximize separation between deposited solder paste to avoid bridging.

Component Placement

BGAs can be picked up and placed using standard pick-and-place (P&P) equipment. Minimum requirements of a P&P system include a vision system to recognize and position the part and a mechanical system to perform P&P operations. The placement accuracy of the system is dependent on either its vision system that locates chip edges or on the individual (pre-taught) bump of the BGA. Using the bump as the placement and orientation reference tends to be accurate but is expensive and time consuming.

Both methods are acceptable since during solder reflow, the BGA aligns due to the self-centering feature of the solder joints. The maximum placement offset allowable during assembly is ±0.150mm in the X and Y directions.

Cleaning

Standard cleaning materials and methods that are acceptable for standards PCBs and components are acceptable for this device. This includes the use of ultrasonic equipment and alcohol based cleaning solvents. Note that flux cleaning depends on the type of flux used. Solder paste with active flux is not recommended due to corrosion issues.

Solder Joint Inspection

The structure of BGAs prohibits direct inspection of all the solder joints. Thus X-ray equipment is necessary for sample monitoring of the solder joint attachment process to identify defects such as bridging, opens, shorts and voids, and to uncover process related problems that may affect all solder joints.

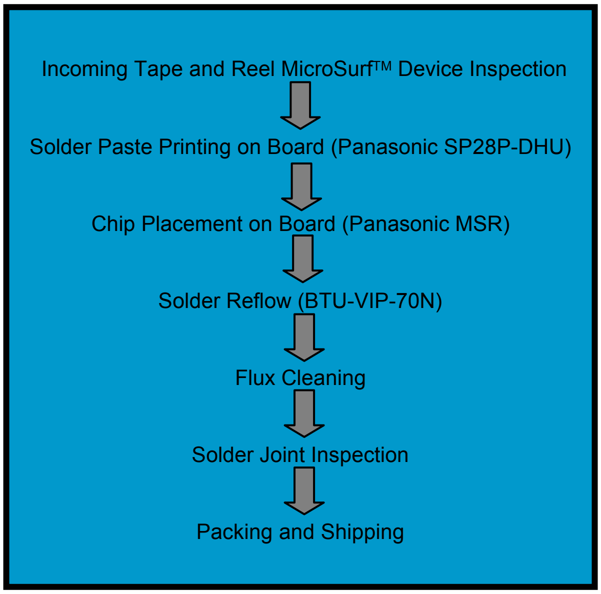
BGA Rework

Following are the key steps necessary to properly rework a BGA assembly:

1. BGA removal uses localized heating similar to original reflow profile using convection nozzle and preheat from the bottom.
2. Once the nozzle temperature reaches the solder reflow temperature, the defective BGA can be removed using tweezers.
3. The pads need to be resurfaced by using a temperature-controlled soldering iron.
4. Gel flux is applied to the pad.
5. A replacement part is picked up using a vacuum needle pick-up tip and placed accurately using a placement jig.
6. Reflow the part using the same convection nozzle and preheat from bottom, matching the original reflow profile.

SMT Process Flow and Equipment

The following steps can be used to assemble the MicroSurf™ onto a PCB.



Paralleling Multiple Devices

For applications requiring more than one device, care must be taken to employ a layout that is both compact, but also maximizes performance. Figure 7 illustrates a potential solution for paralleling four devices. In this implementation, all four terminals are accessed from the top layer. Vias are used extensively outside the boundaries of the device, reducing thermal resistance. Also, since the source connection is made from the bumps to the second layer using vias, this terminal is brought back to the top layer using an additional array of vias. The second metal layer is also used to facilitate the connection to the Drain-sense terminal.

Board Construction notes:

1. Layers 1 & 2 to start with 5 micron foil and plated to 2 oz (0.071mm). Layers 3 is standard 2 oz Cu (0.071mm).
2. The Pre-preg layers between 1-2 and 2-3 are single sheet FR-4 laminate, pressed out to 0.083mm nominal.
3. The Anti-pad diameter on layer 2 will be 0.45 mm for adequate clearance.
4. Blind via diameter between layers 1-2 will be 0.16mm.
5. Blind via diameter between layers 1-3 will be 0.16mm.
6. Via plating conditions should be 0.01mm minimum, and may be plated shut between layers 2-3.

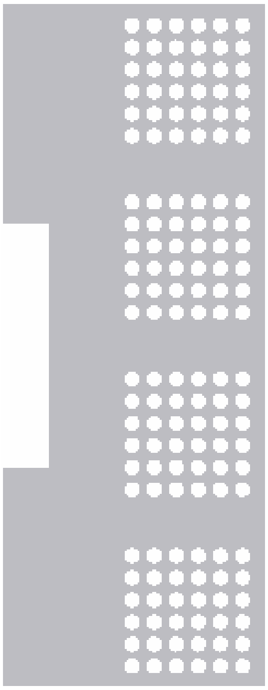


Figure 7a. Solder Mask

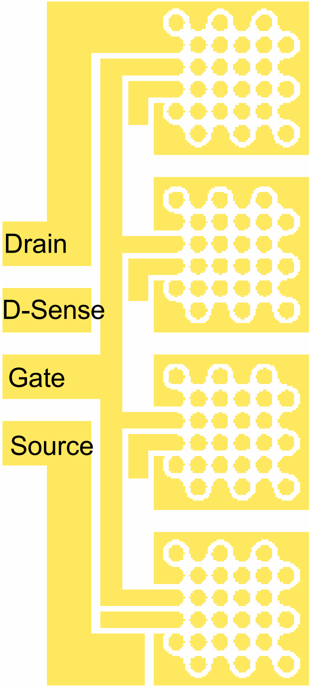


Figure 7b. Metal Layer 1

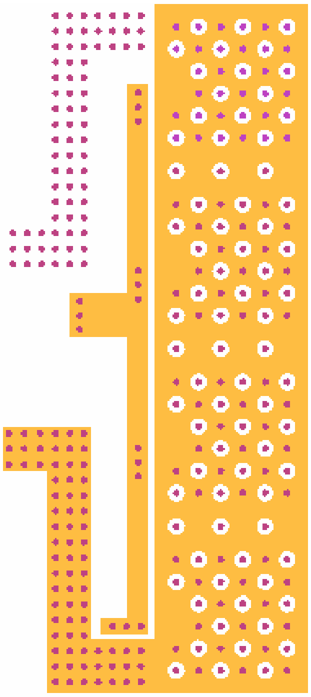


Figure 7c. Metal Layer 2 and Vias between 1-2

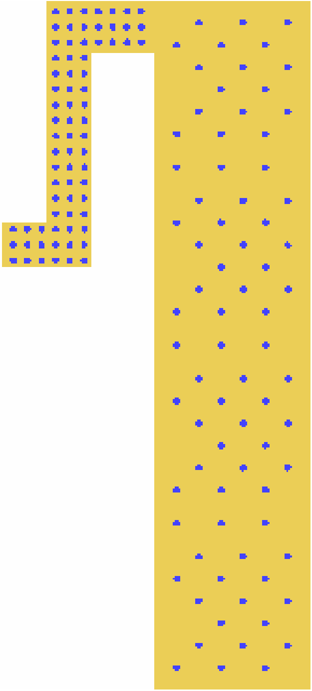


Figure 7d. Metal Layer 3 and Vias between 1-3

Single Layer PCB Layout

Figure 8 illustrates a potential layout solution for a single layer PCB. Thermal resistances and voltage drops will be higher comparing to the multilayer board approach.

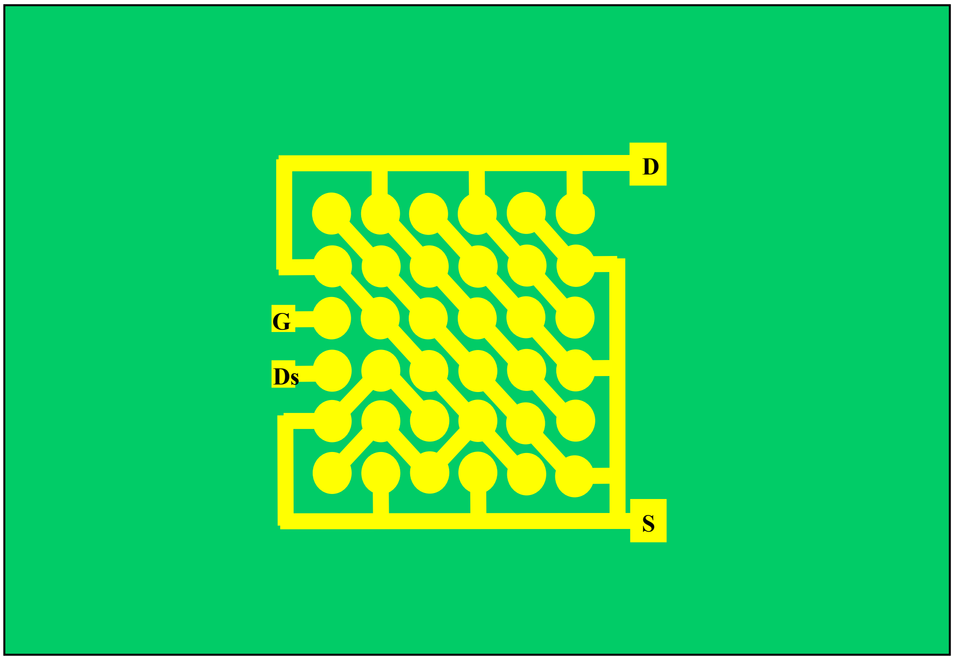


Figure 8. Single Layer PCB Layout